ICL5101

Resonant controller IC with PFC for LED driver

Datasheet

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Power Management & Multimarket

Resonant controller IC with PFC for LED driver

Product highlights

- Supports universal input and wide output range
- Low count of external components supporting small form factors and improved reliability
- All parameters set by simple resistors only
- Supports outdoor use by extended junction temperature range from -40 °C to +125 °C
- Stable low load operation mode down to 0.1 % of nominal power rating
- Comprehensive set of protection features incl. external over temperature protection and capacitive load protection to increase system safety
- Ultra-fast time to light < 200 ms
- Power Factor Correction > 99 %, THD < 5 %
- High efficiency up to 94 %

PFC feature set

- PFC in CritCM mode during nominal load and DCM mode in low load condition down to 0.1 % for operation without audible noise
- Improved compensation for low THD of AC input current even in DCM operation
- Adjustable PFC current limitation

Resonant half bridge feature set

- Fully integrated 650 V high-side driver
- Self-adaptive dead time control of the integrated half bridge driver 500 ns – 1.0 µs
- Detection of capacitive operation, overload, short circuitry and output overvoltage
- Improved operation control in magnetic saturation during start-up
- Advanced error detection control

PG-DSO-16

Applications

- LED driver, e.g. commercial or residential lighting systems > 50 W
- Integrated electronic control gear for LED luminaires

Description

The LED Resonant controller ICL5101 is designed to control resonant converter topologies. The PFC stage operates in CrCM and DCM mode, supporting low load conditions. Integrated high and low side drivers assure a low count of external components, enabling small form factor designs.
ICL5101 parameters are adjusted by simple resistors only, this being the ideal choice to ease the design-in process. A comprehensive set of protection features ensures that the LED driver detects fault conditions, protecting both the LED driver and the LED load. Figure 1 shows a typical application circuit of a 110 W constant voltage LED driver.

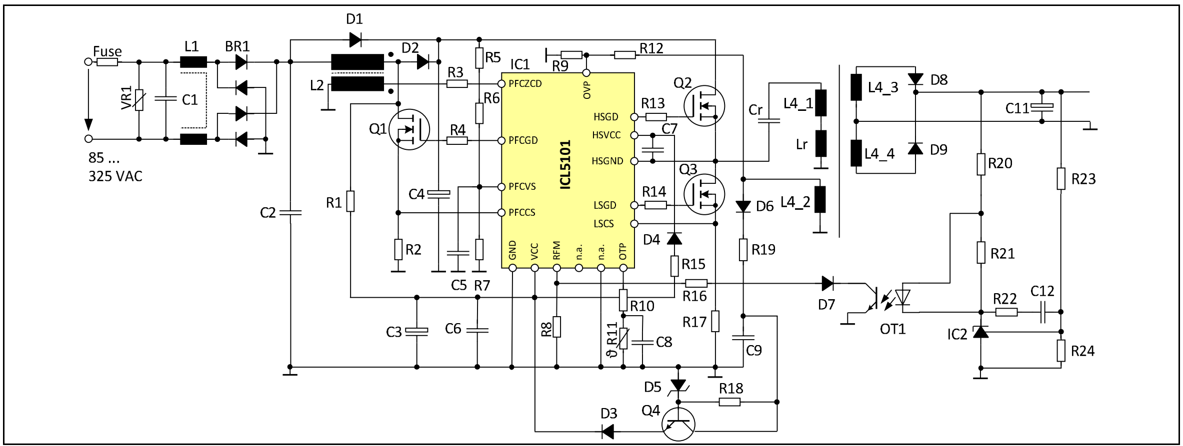

Figure 1. Typical Application

Product type	Package
ICL5101	PG-DSO-16

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1 Pin Configuration and Description

The pin configuration is shown in **Figure 2** and **PIN Functionality** Table 1. The pin functions are described below.

1.1 PG-DSO-16 Package

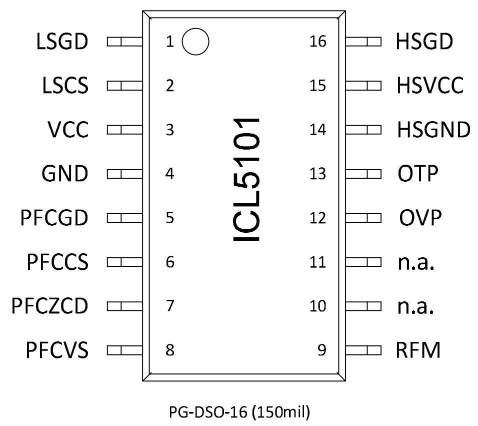


Figure 2. Pin Configuration

1.2 PIN Configuration for PG-DSO-16

Symbol	Pin	Function
LSGD	1	Low-side gate drive
LSCS	2	Low-side current sense signal
VCC	3	Chip supply voltage
GND	4	IC GND
PFCGD	5	PFC gate drive
PFCCS	6	PFC current sense signal
PFCZCD	7	PFC zero crossing detection
PFCVS	8	PFC voltage sensing
RFM	9	Set RUN frequency
n.a.	10	NOT APPLICABLE: Leave PIN OPEN
n.a.	11	NOT APPLICABLE: SET to GND
OVP	12	Overvoltage protection of secondary output
OTP	13	Over temperature protection
HSGND	14	High-side GND
HSVCC	15	High-side supply voltage
HSGD	16	High-side gate drive

1.3 PIN Set-Up

The PIN set-up of ICL5101 is shown in Figure 3.

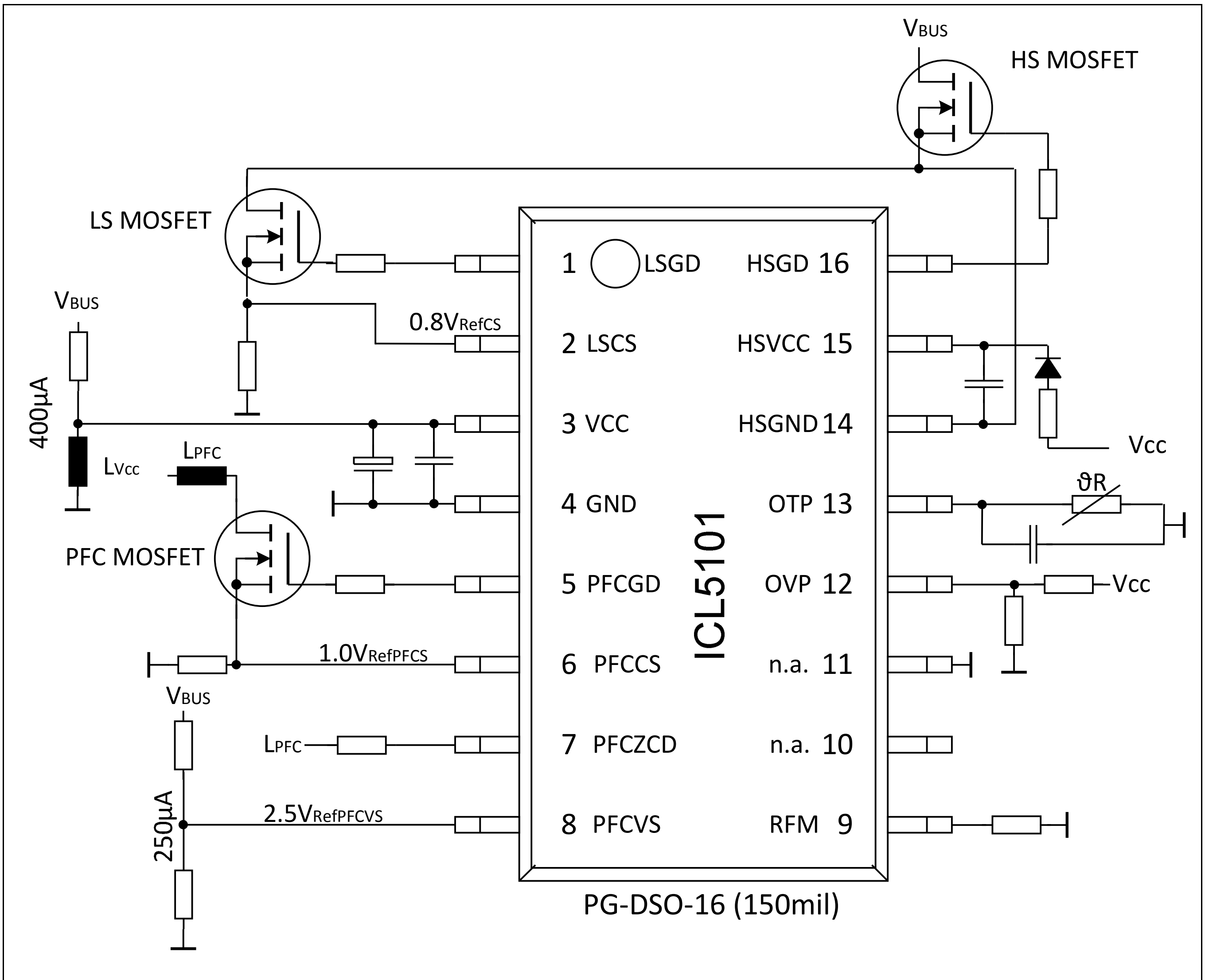


Figure 3. PIN Set-Up

The schematic in Figure 3 shows a typical PIN set-up for a PFC / LLC converter

1.4 PIN Functionality

Table 1. Pin Definitions and Functions

Symbol	Pin	Function
LSGD	1	**Low-side gate drive** The gate of the low-side MOSFET in an RESONANT inverter topology is controlled by this pin. There is an active L-level during UVLO (undervoltage lockout) and a limitation of the max H-level at 11.0 V during normal operation. In order to turn on the MOSFET softly (with a reduced di_{DRAIN}/dt), the gate voltage rises typically within 245 ns from L-level to H-level. The fall time of the gate voltage is less than 50 ns in order to turn off quickly. This measure produces different switching speeds during turn-on and turn-off as it is usually achieved with a diode parallel to a resistor in the gate drive loop. It is recommended to use a resistor of typically 10 Ω between the drive pin and gate in order to avoid oscillations and in order to shift the power dissipation when discharging the gate capacitance into this resistor. The typical dead time between the LSGD signal and HSGD signal is self-adapting between 500 ns and 1.0 µs.
LSCS	2	**Low-side current sense signal** This pin is directly connected to the shunt resistor, which is located between the source terminal of the low-side MOSFET of the inverter and ground. Internal clamping structures and filtering measures allow sensing of the source current for the low side inverter MOSFET without additional filter components. There is a first threshold of 0.8 V. If this threshold is exceeded for longer than 500 ns during run mode, an inverter overcurrent is detected, which causes a latched shutdown of the IC. The saturation control is activated if the sensed slope at the LSCS pin reaches typical values of 205 mV/µs ± 25 mV/µs and exceeds the 0.8 V threshold. The saturation regulator is now continuously monitored by the LSCS pin during saturation control and extended saturation control mode. In saturation control the regulator is designed to handle a choke operation in saturation. If the sensed current signal exceeds a second threshold of 1.6 V for longer than 500 ns before entering the run mode, the IC changes over into a latched shutdown. There are further thresholds active at this pin during run mode that detect capacitive mode operation. A voltage level below -50 mV indicates faulty operation (operation below resonance). A second threshold at 2.0 V senses even short over currents during turn-on of the high-side MOSFET such as is typical for reverse recovery currents of a diode. If one of these comparator thresholds indicates incorrect operating conditions for longer than 620 µs (overcurrent / operation below resonance) in run mode, the IC turns off the gates and changes to fault mode due to detected capacitive mode operation (non-zero voltage switching). The threshold of -50 mV is also used to adjust the dead time between turn-off and turn-on of the RESONANT drivers in a range of 500 ns to 1.0 µs during all operating modes.
VCC	3	**Chip supply voltage** This pin provides the power supply of the ground-related section of the IC. There is a turn-on threshold at 14.0 V and a UVLO threshold at 10.6 V. The upper supply voltage level is 17.5 V. There is an internal zener diode clamping V_{CC} at 16.3 V (at I_{VCC} = 2 mA typically). The maximum zener current is internally limited to 5 mA. An external zener diode is required for higher current levels. Current consumption during UVLO and during fault mode is less than 170 µA. A ceramic capacitor close to the supply and GND pin is required in order to act as a low-impedance power source for gate drive and logic signal currents. In the event of a short interruption to the mains supply, feed the start-up current (160 µA) from the bus voltage.

Symbol	Pin	Function
GND	4	**IC GND** This pin is connected to ground and represents the ground level of the IC for the supply voltage, gate drive and sense signals.
PFCGD	5	**PFC gate drive** The gate of the MOSFET in the PFC preconverter designed in boost topology is controlled by this pin. There is an active L-level during UVLO and a limitation of the max H-level at 11.0 V during normal operation. In order to turn on the MOSFET softly (with a reduced di_{DRAIN}/dt), the gate drive voltage rises within 245 ns from L-level to H-level. The fall time of the gate voltage is less than 50 ns in order to turn off quickly. A resistor of typically 10 Ω is recommended between the drive pin and gate in order to avoid oscillations and in order to shift the power dissipation when discharging the gate capacitance into this resistor. The PFC section of the IC controls a boost converter as a PFC preconverter in discontinuous conduction mode (DCM). Typically, the control starts with gate drive pulses with a fixed on-time of typically 4.0 µs at V_{ACIN} = 230 V, increasing up to 24 µs and with an off-time of 47 µs. As soon as sufficient zero current detector (ZCD) signals are available, the operation mode changes from fixed frequency operation to operation with variable frequency. The PFC works in critical conduction mode operation (CritCM) when rated and/or medium load conditions are present. That means triangular-shaped currents in the boost converter choke without gaps and variable operating frequency. During low load (detected by an internal compensator) we obtain operation with discontinuous conduction mode (DCM) – that means triangular-shaped currents in the boost converter choke with gaps when reaching the zero current level and variable operating frequency in order to avoid steps in the consumed line current.
PFCCS	6	**PFC current sense signal** The voltage drop across a shunt resistor located between the source of the PFC MOSFET and GND is sensed with this pin. If the level exceeds a threshold of 1.0 V for longer than 200 ns, the PFC gate drive is turned off as long as the zero current detector (ZCD) enables a new cycle. If no ZCD signal is available within 52 µs after turn-off of the PFC gate drive, a new cycle is initiated from an internal start-up timer.
PFCZCD	7	**PFC zero crossing detection** This pin senses the point of time when the current through the boost inductor becomes zero during the off-time of the PFC MOSFET in order to initiate a new cycle. The moment of interest appears when the voltage of the separate ZCD winding changes from positive to negative level, which represents a voltage of zero at the inductor windings and therefore the end of current flow from the lower input voltage level to the higher output voltage level. There is a threshold with hysteresis, 1.5 V for increasing level, 0.5 V for decreasing level, which detects the change in inductor voltage. A resistor connected between the ZCD winding and PIN 7 limits the sink and source current of the sense pin when the voltage of the ZCD winding exceeds the internal clamping levels (typically 6.3 V and -2.9 V @ 5 mA) of the IC. If the sensed voltage level of the ZCD winding is not sufficient (e.g. during start-up), an internal start-up timer will initiate a new cycle every 52 µs after turn-off of the PFC gate drive. The source current out of this pin during the on-time of the PFC-MOSFET indicates the voltage level of the AC supply voltage. During low input voltage levels, the on-time of the PFC-MOSFET is enlarged in order to minimize gaps in the line current during zero crossing of the line voltage and improve the THD (Total Harmonic Distortion) of the line current. Optimization of the THD is possible by trimming of the resistor between this pin and the ZCD winding in combination with the inductance and used PFC MOSFET.

Symbol	Pin	Function
PFCVS	8	**PFC voltage sensing** The intermediate circuit voltage (bus voltage) at the smoothing capacitor is sensed by a resistive divider at this pin. The internal reference voltage for the rated bus voltage is 2.5 V. There are further thresholds at 0.3125 V (12.5 % of the rated bus voltage) for detection of open control loop and at 1.875 V (75 % of the rated bus voltage) for detection of undervoltage, and at 2.725 V (109 % of the rated bus voltage) for detection of overvoltage. The overvoltage threshold operates with a hysteresis of 100 mV (4 % of the rated bus voltage). The bus voltage is sensed at 95 % (2.375 V) for detection of a successful start-up. It is recommended to use a small capacitor between this pin and GND as a spike suppression filter. In run mode, PFC overvoltage stops the PFC gate drive within 5 µs. As soon as the bus voltage is less than 105 % of the rated level, the gate drives are enabled again. If the overvoltage lasts for longer than 625 ms, an inverter overvoltage is detected and turns off the inverter gate drives also. This causes a power-down and a power-up when $V_{BUS} < 109$ %. A bus under- ($V_{BUS} > 75$ %) or inverter overvoltage during run mode is handled as FAULT BUS. In this situation the IC changes to power-down mode and generates a delay of 100 ms with an internal timer. Then start-up conditions are checked and if valid, a further start-up is initiated. If start-up conditions are not valid, a further delay of 100 ms is generated. This procedure is repeated a maximum of seven times. If a start-up is successful within these seven cycles, the situation is interpreted as a short interruption of the mains supply.
RFM	9	**Set minimum RUN frequency** A resistor from this pin to ground sets the operating frequency of the inverter during run mode. The typical run frequency range is 20 kHz to 120 kHz @ -40°C and 130kHz @ - 25°C. The set resistor R_RFM can be calculated based on the run frequency f_{RFM} according to the equation: $R_{RFM} = \frac{5 \cdot 10^8 \Omega Hz}{f_{RUN}}$
n.a.	10	NOT Applicable: Leave PIN Open
n.a.	11	NOT Applicable: SET to IC GND as short as possible
OVP	12	**Over voltage protection of OUTPUT Voltage** In order to prevent overvoltage at the output stage – in the case of a floating LED –overvoltage protection at pin 12 can be activated. Use a resistor and a ceramic capacitor connected to the auxiliary winding in order to sense the voltage level at the auxiliary winding. During run mode, the auxiliary winding is monitored by a sensing current proportional to the auxiliary voltage. If the peak-to-peak voltage at this pin exceeds a threshold of 210 µApp for longer than 620 µs, overvoltage is detected. This function can be disabled by setting pin 12 to GND.
OTP	13	**Over temperature protection** In order to prevent over temperature of the system, activate the over temperature protection at the OTP pin. Use a temperature-dependent resistor and a ceramic capacitor connected to GND for activation. There is a threshold of 3.2 V at the OTP pin during active run mode. If the voltage rises above this threshold for longer than 620 µs, the IC detects over temperature and changes to the latched fault mode. The latch mode is ended automatically by power-up or UVLO. This function can be disabled by setting pin 13 to GND.

Symbol	Pin	Function
HSGND	14	**High-side GND** This pin is connected to the source terminal of the high-side MOSFET, which is also the node of high-side and low-side MOSFET. This pin represents the floating ground level of the high-side driver and the high-side supply.
HSVCC	15	**High-side supply voltage** This pin provides the power supply of the high-side ground-related section of the IC. An external capacitor between pins 14 and 15 acts like a floating battery, which has to be recharged cycle by cycle via a high-voltage diode from the low-side supply voltage during the on-time of the low-side MOSFET. A UVLO threshold with hysteresis enables the high-side section at 10.4 V and disables it at 8.6 V.
HSGD	16	**High-side gate drive** The gate of the high-side MOSFET in an RESONANT inverter topology is controlled by this pin. There is an active L-level during UVLO and a limitation of the max H-level at 11.0 V during normal operation. The switching characteristics are the same as described for LSGD (pin 2). It is recommended to use a resistor of about 10 Ω between the drive pin and gate in order to avoid oscillations and in order to shift the power dissipation when discharging the gate capacitance into this resistor. The dead time between the LSGD signal and HSGD signal is self-adapting between 500 ns and 1.0 µs (typically).

2 Functional Description

The functional description provides an overview of the integrated functions, features and their relationships. The parameters and equations provided are based on typical values at T_A = 25 °C. The corresponding minimum and maximum values are shown in the Electrical Characteristics.

2.1 Introduction

The ICL5101 is a high-performance mixed-signal controller for LED and SMPS applications. The IC is designed for a Power Factor Correction (PFC) close to 1, low THD below 5 %, a maximum efficiency up to 94 % PLUS and a minimal design-in phase in wide and narrow range designs. Furthermore, all parameters are valid in an extended temperature range from –40 °C up to 125 °C – especially frequency and timing. The controller utilizes a variety of protection features, including saturation control during start-up of the RESONANT converter, adjustable over temperature, along with open and short load conditions.

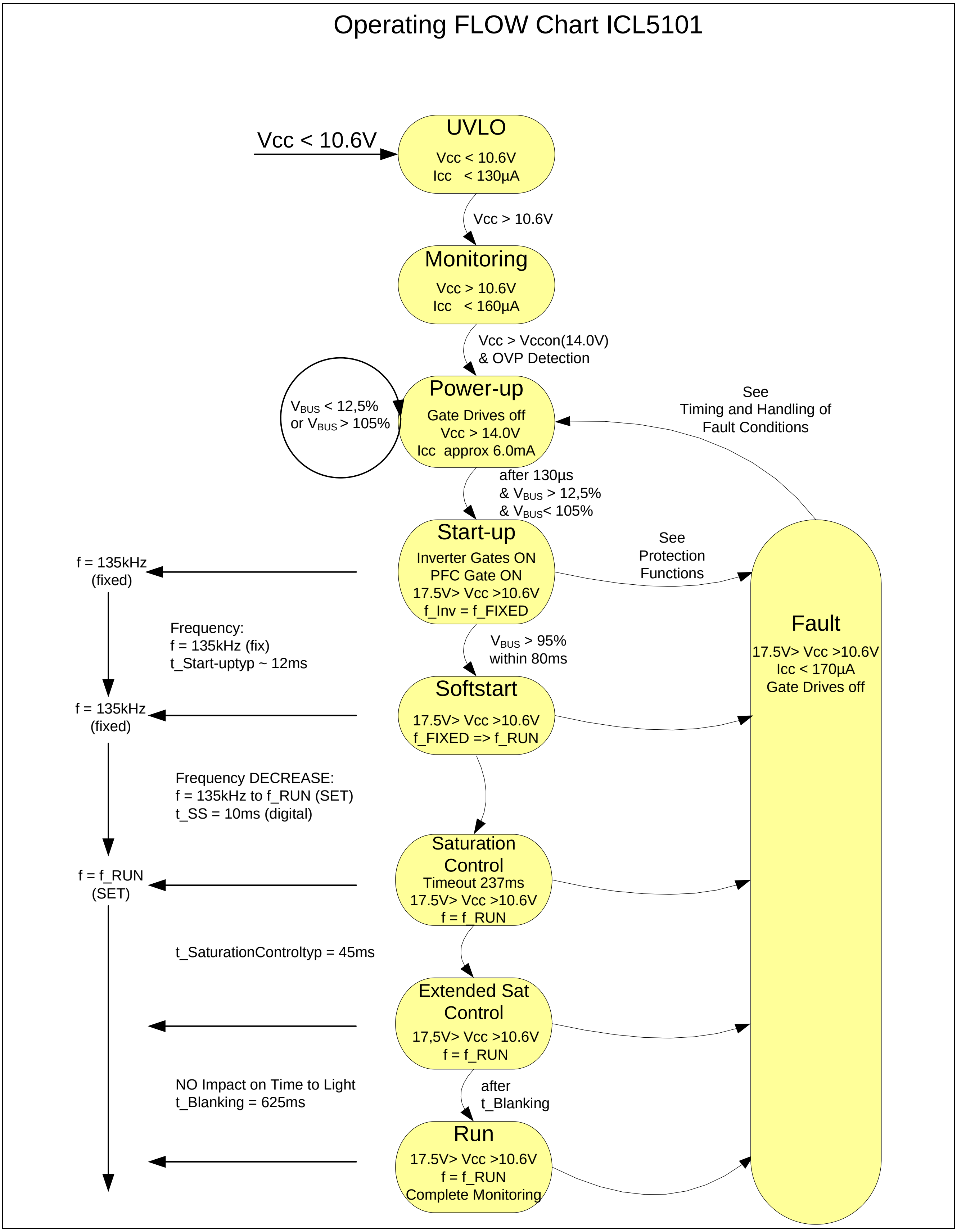


Figure 4. Operating Flowchart for LED Applications

Start-Up
The device is powered through the VCC pin. All device supply voltages are internally generated from VCC voltage. Figure 5. Typical Start-Up Procedurebelow shows a typical start-up procedure of the device. The following subsections describe the phases in detail.

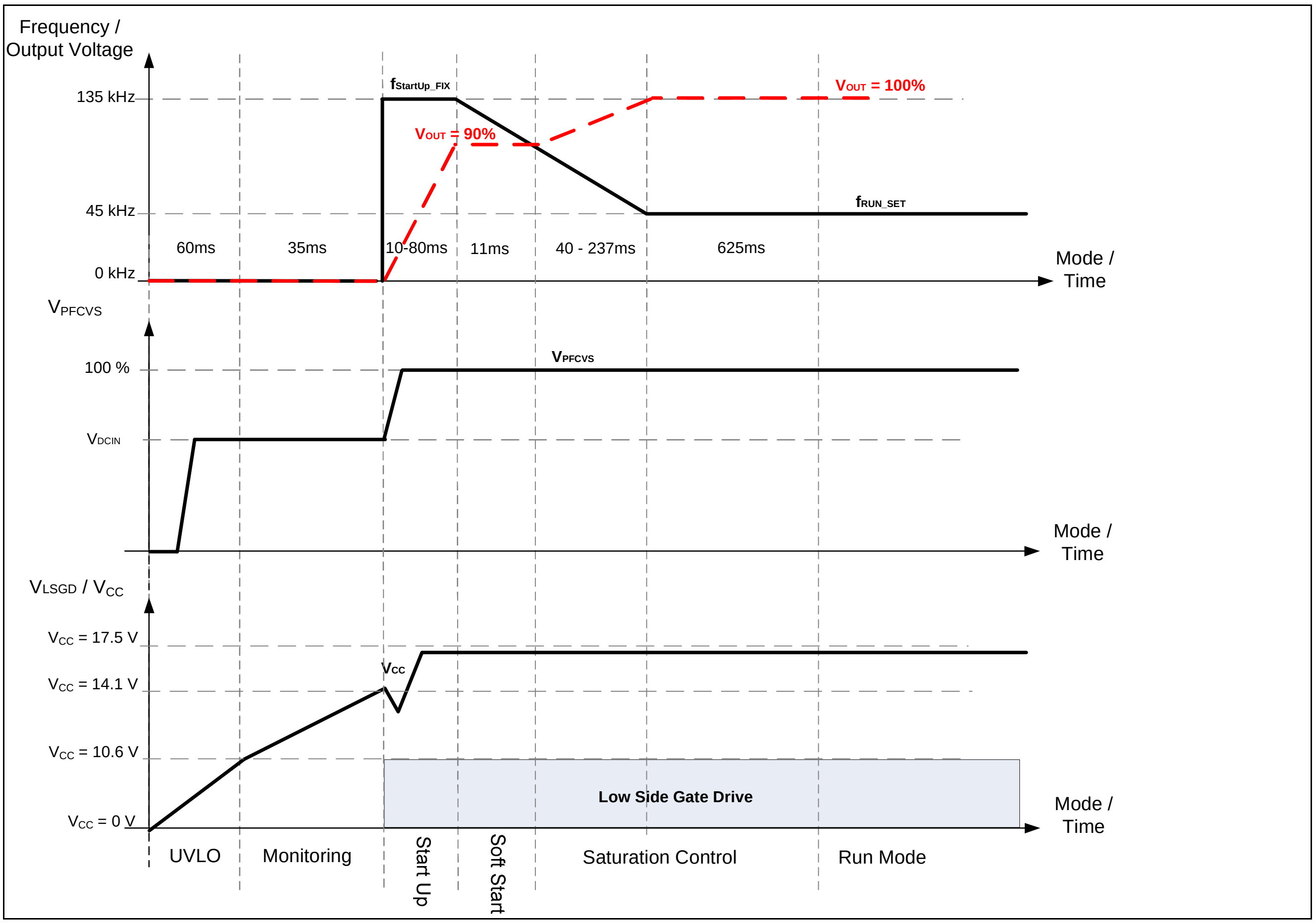


Figure 5. Typical Start-Up Procedure

2.1.1 UVLO to Soft Start

This section describes the operating flow from UVLO to soft start in detail – Figure 6. Start-Up Procedure from UVLO to Soft Start. The control of the LED ballast is able to start the operation in less than 100 ms (Time to Light IC is in active mode). This is achieved by the low current consumption during UVLO (I_{VCC} = 130 µA) and start-up hysteresis (I_{VCC} = 160 µA – defines the start-up resistor) phases. The chip supply stage of the IC is protected against overvoltage via an internal Zener clamping network, which clamps the voltage at 16.3 V and allows a current of 2.5 mA. For clamping currents above 2.5 mA, an external Zener diode from VCC to GND is required.

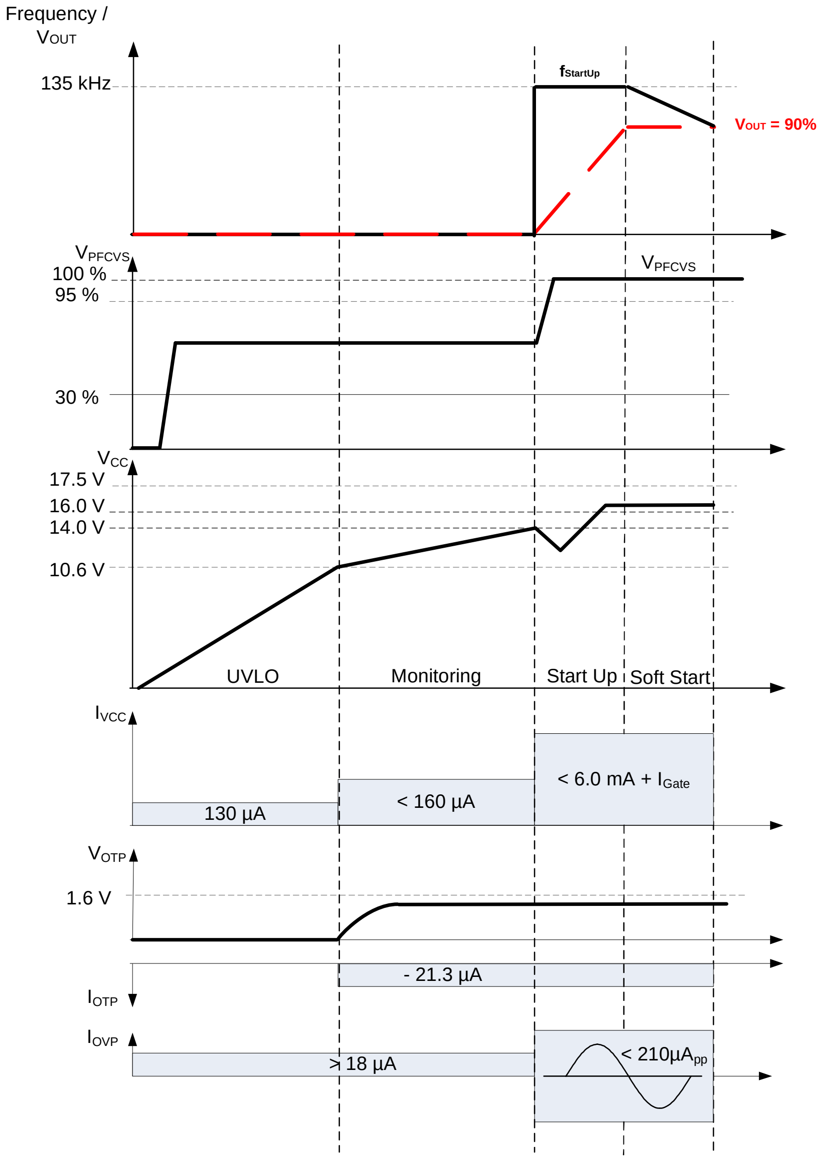


Figure 6. Start-Up Procedure from UVLO to Soft Start

If V_{CC} exceeds the 10.6 V level and stays below 14.0 V (start-up hysteresis), the IC checks whether the pcb temperature is experiencing overtemperature or an output overvoltage is present. Overtemperature is checked from a source current of typically I_{OTP3} = - 21.3 µA out of pin 13 OTP (I_{OTP}). This current produces a voltage drop of V_{OTP} < 1.6 V (temperature is ok). Overtemperature is detected if the voltage at the OTP pin exceeds the V_{OTP} > 1.6V threshold (V_{OTP}).
The output overvoltage is checked by a current of typically I_{OVP} > 12 µA via resistors R12 into the OVP pin 12. Output overvoltage is detected if there is no sink current into the OVP pin. This causes a higher source current out of the OTP pin (typically 42.6 µA / 35.4 µA) in order to exceed V_{OTP} > 1.6 V. In the case of over temperature or overvoltage, the IC keeps monitoring until there is an adequate voltage from the OTP or OVP pin.

When V_{CC} exceeds the 14.0 V threshold – by the end of the start-up hysteresis – the IC waits for 80 µs and senses the bus voltage. When the rated bus voltage is in the corridor of 12.5 % < $V_{BUSrated}$ < 105 %, the IC powers up. The IC initiates an UVLO when the chip supply voltage is below V_{CC} < 10.6 V. As soon as the condition of a power-up is fulfilled, the IC starts the inverter gate operation with an internal fixed start-up frequency of 135 kHz. The PFC gate drive starts with a delay of app. 300 µs. Then the bus voltage will be checked for a rated level above 95 % for a duration of 80 ms. Now, the IC enters the soft start phase and shifts the frequency from the internal fixed start-up frequency of 135 kHz down to the set RUN frequency.

2.1.2 Soft Start to Run Mode

This section describes the operating flow from soft start to run mode in detail. After the soft start phase is finished, the saturation control phase is entered.

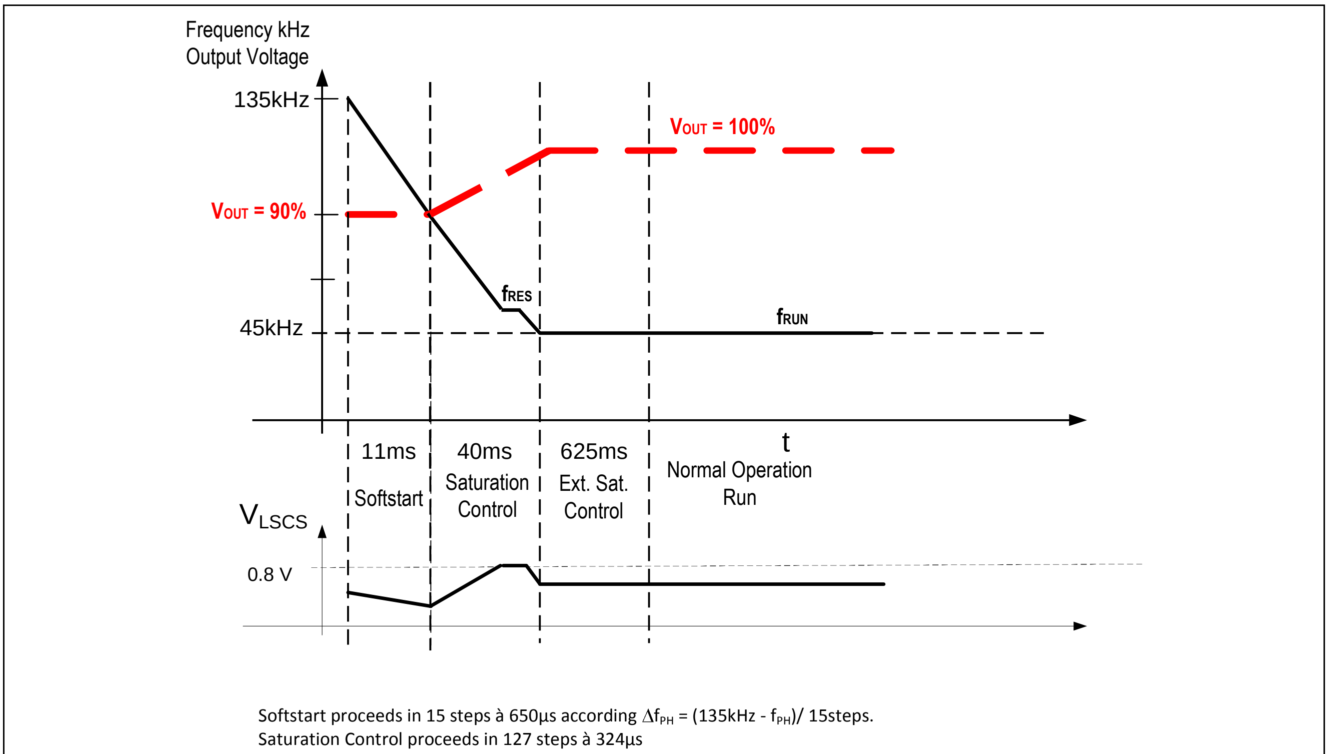


Figure 7 Start-Up Procedure from Soft Start to Run Mode

During saturation control (Figure 7 Start-Up Procedure from Soft Start to Run Mode), the operating frequency of the inverter is shifted downward in t_{typ} = 40 ms to the run frequency set by a resistor at the pin RFM to GND. The saturation control is activated if the sensed slope at the LSCS pin reaches typically 205 mV/µs ± 25 mV/µs and exceeds the 0.8 V threshold. This stops the frequency decreasing and signifies waiting for an adequate output voltage. The saturation control is now continuously monitored by the LSCS pin. The maximum duration of the saturation control procedure is limited to 237 ms. If there is still saturation within this time frame, the saturation control is disabled and the IC changes over to the latched fault mode. Furthermore, in order to reduce the choke size, the saturation control is designed to operate with a choke in magnetic saturation of the RESONANT during start-up. For an operation in magnetic saturation during saturation control mode, the voltage at the shunt at the LSCS pin 2 has to be V_{LSCS} = 0.80 V when the output voltage is reached. If the saturation control mode is successfully passed, the IC enters the extended saturation mode The extended saturation mode is a safety mode used in order to prevent a malfunction of the IC due to an instable system. After 625 ms of extended saturation mode, the IC changes to the run mode (Figure 7 Start-Up Procedure from Soft Start to Run Mode). The run mode monitors the complete system regarding bus over- and undervoltage, open loop, overcurrent of PFC and/or inverter, output overvoltage, overtemperature and capacitive load operation.

2.2 Detection Stage

2.2.1 Detection of Overtemperature

Force a shut-off of the IC due to over temperature by using a PTC to GND on pin 11. In the event of an over temperature of the system (in run mode), the current out of the OTP pin 11 I_{OTP3} = - 21.3 µA charges up a capacitor. If the voltage at the OTP pin 11 exceeds the V_{OTP3} = 3.2V threshold, the controller detects an over temperature and stops the gate drives after a delay of t = 620µs set by an internal timer. The system restarts automatically. The possibility of a latch of the system is happen when it cools down and heat up within 200ms. When system is too hot before startup, the system prevents a power up.

2.2.2 Detection of Output Overvoltage

Overvoltage is detected by measuring the peak levels of the voltage at the AUX winding via an AC current fed into the OVP pin 12. If the sensed AC current exceeds 210 μA_{PP} for longer than 620 µs, the status of overvoltage is detected. The OVP fault results in a latched power-down mode (after trying a single restart). The controller continuously monitors the status until the overvoltage status changes.

2.2.3 Detection of Capacitive Mode Operation

RESONANT converter designs should avoid working in capacitive mode operation –not even under abnormal conditions. ICL5101 provides capacitive mode operation detection and latch-off of the system after a single restart for error verification. Resonant converters work in capacitive mode when their switching frequency falls below a critical value. This depends on the loading condition and the input-to-output ratio. They are especially prone to enter capacitive mode when the input voltage is lower than the minimum specified and/or the output is overloaded or shorted. In order to prevent a malfunction in the area of capacitive load during run mode due to certain deviations from the normal load, the IC senses only via the LSCS pin 2.

Capacitive load operation is detected if the voltage at the LSCS pin drops below a second threshold of V_{LSCS} = – 50 mV directly before the high-side MOSFET is turned on or exceeds a third threshold of V_{LSCS} = 2.0 V during ON switching of the high-side MOSFET (see Figure 8 Capacitive Mode Operation). If this overcurrent is present for longer than 620 µs, the IC results a latched power-down mode after trying a single restart.

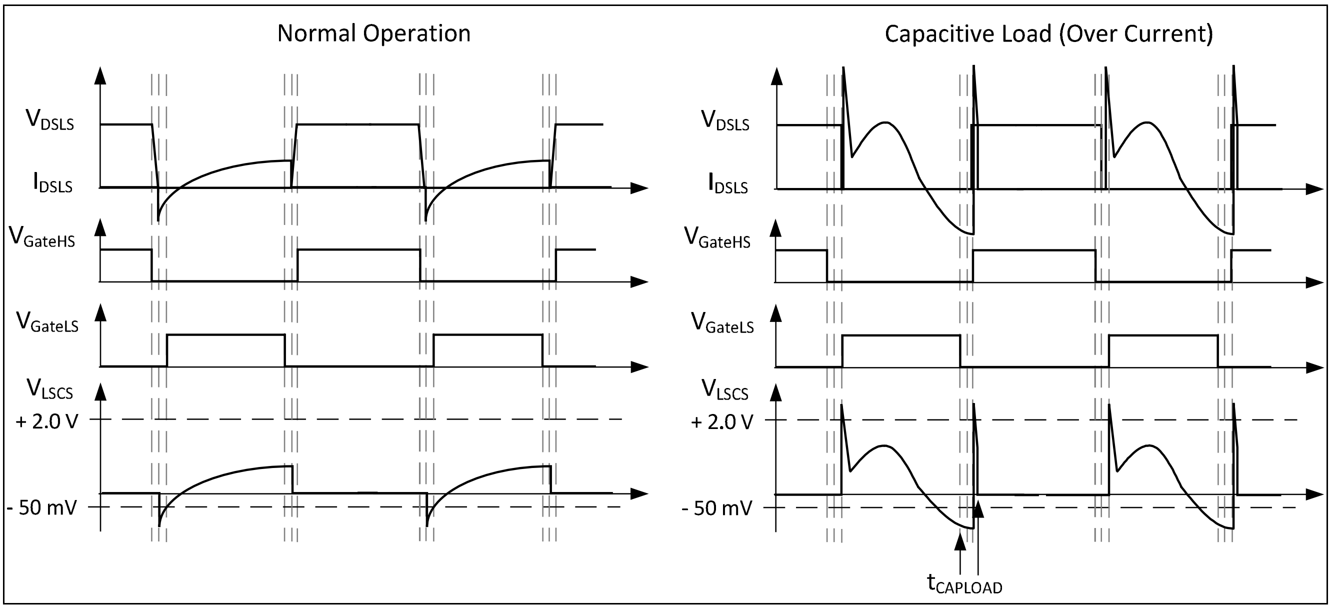


Figure 8 Capacitive Mode Operation

2.2.4 Self-Adapting Dead Time during Gate Drive Activity between HS and LS

The dead time between the turn OFF and turn ON of the RESONANT drivers is self-adapting and is detected by means of switch-off of the high-side MOSFET and the –50 mV threshold of the LSCS voltage (in Figure 9 Dead Time ON and OFF of the Inverter Gate Drivers). The typical range of the dead time adjustment is 500 ns up to 1.0 µs during all operating modes. The start of the dead time measurement is the OFF switching of the high-side MOSFET. The dead time measurement finishes when V_{LSCS} drops below -50 mV for longer than typically 300 ns (internal fixed propagation delay). This time will be stored (= stored dead time) and the low-side gate driver switches ON. The high-side gate driver turns ON again after OFF switching of the low-side switch and the stored dead time.

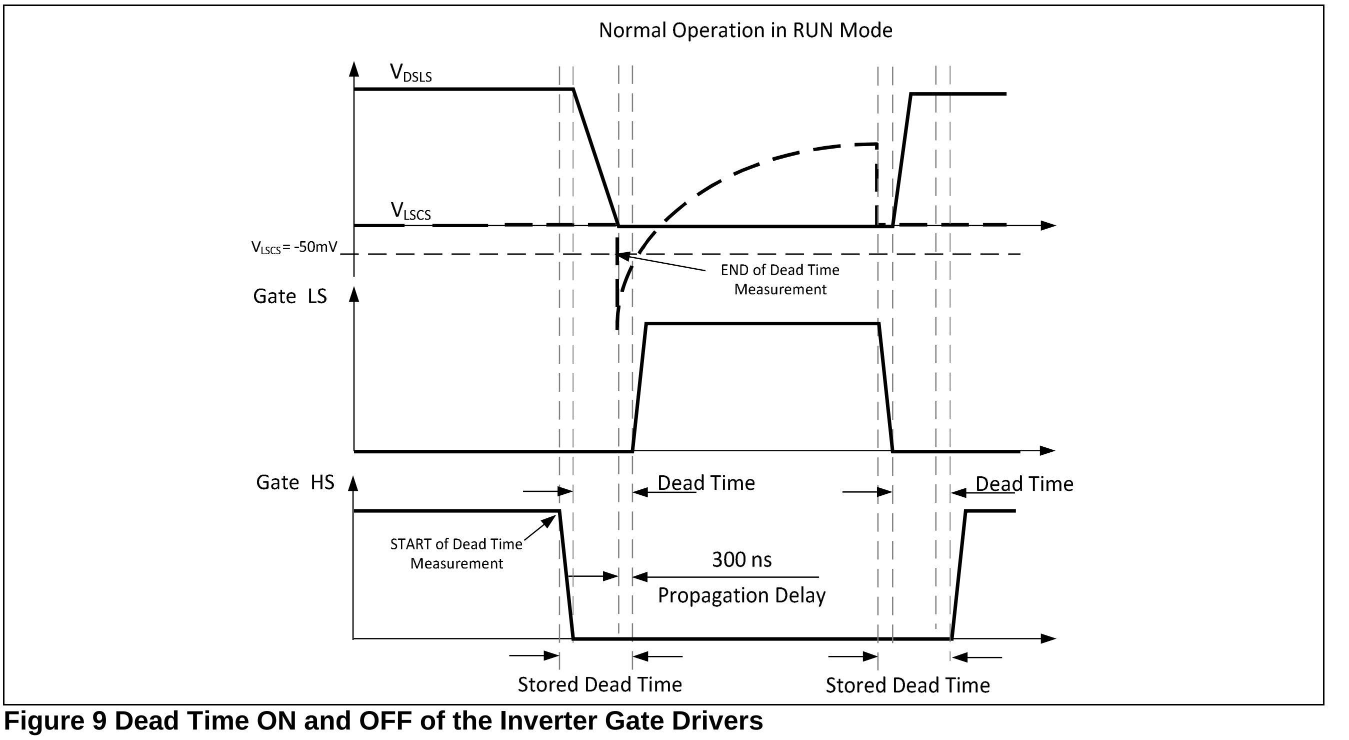


Figure 9 Dead Time ON and OFF of the Inverter Gate Drivers

2.2.5 Short Term Bus Undervoltage

Short-term PFC bus undervoltage (Figure 10 Bus Undervoltage – Short) is detected if the duration of the undervoltage does not exceed 800 ms (timer remains below t < 800 ms). In this case, the PFC and inverter drivers are immediately switched off and the controller continuously monitors the status of the bus voltage in a latched power-down mode (I_{CC} < 170 µA). If the signal at the OVP PIN exceeds 18 µA and the rated bus voltage is above 12.5 % while the timer is below t < 800 ms, the controller restarts from power-up. The timer resets to 0 when entering the run mode.

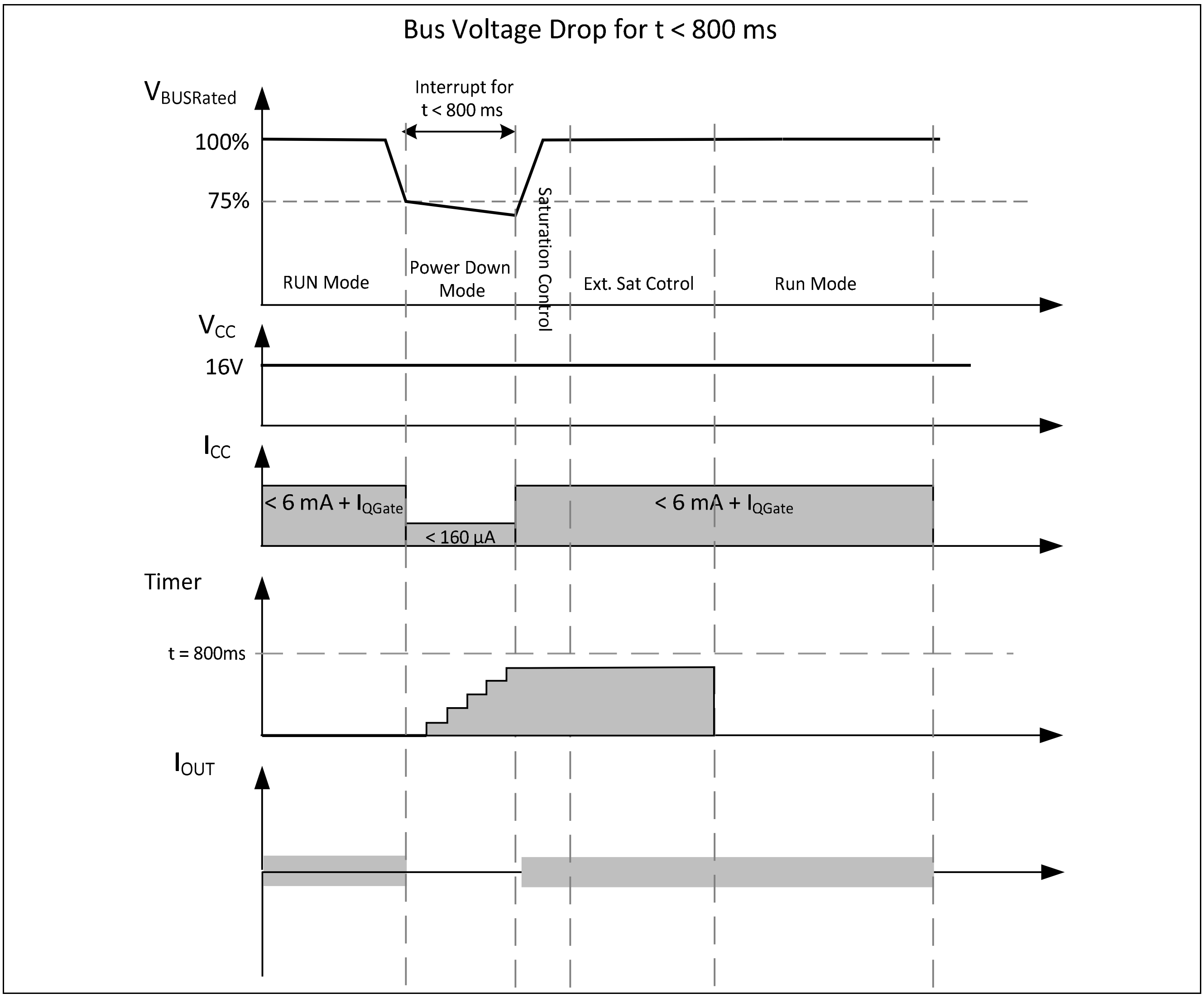


Figure 10 Bus Undervoltage – Short

2.2.6 Long-Term Bus Undervoltage

If the duration of the bus undervoltage exceeds t > 800 ms (see Figure 11 Bus Undervoltage – Long), the controller forces an undervoltage lock-out (UVLO). The chip supply voltage drops below V_{CC} = 10.6 V and the chip supply current is below I_{CC} < 130 µA. When the Vcc voltage exceeds the 10.6 V threshold again, the IC current consumption is below I_{CC} < 160 µA. In this case, the controller resets the timer and restarts with the full start-up procedure, including monitoring, power-up, start-up, soft start, saturation control, extended saturation mode and run mode.

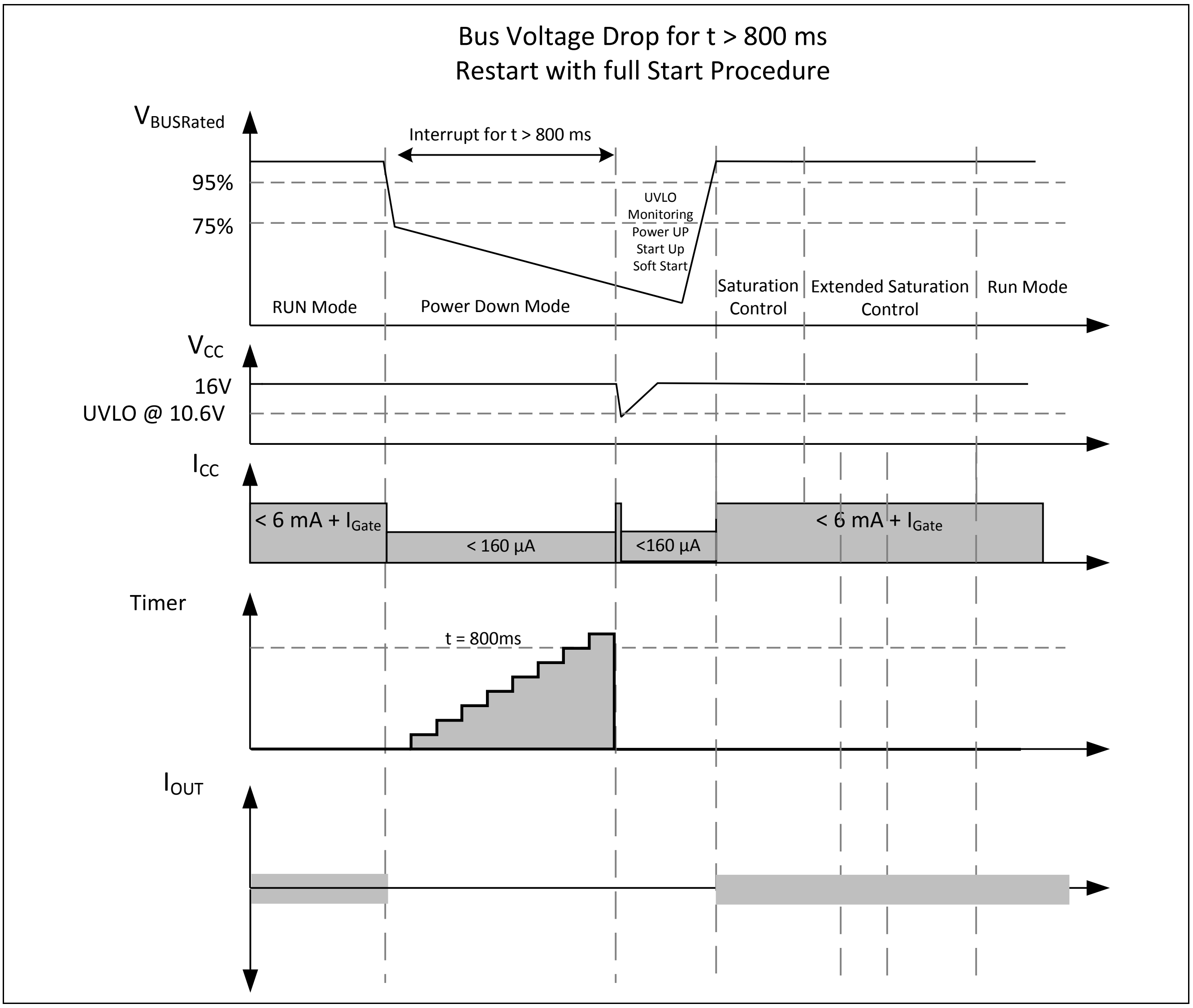


Figure 11 Bus Undervoltage – Long

2.3 PFC Preconverter

2.3.1 Operation Modes of the PFC Converter

The digitally controlled PFC preconverter starts with an internally fixed ON time of typically t_{ON} = 4.0µs and variable frequency. The ON time is increased every 280 µs (typical) up to a maximum ON time of 24 µs. The control switches quite immediately from discontinuous conduction mode (DCM) to critical conduction mode (CritCM) as soon as a sufficient ZCD signal becomes available. The frequency range in CritCM is 22 kHz up to 500 kHz, depending on the power (Figure 12 PFC DCM / CritCM vs Power and ON Time) with a variation in the ON time of 24 µs > t_{ON} > 0.5µs.

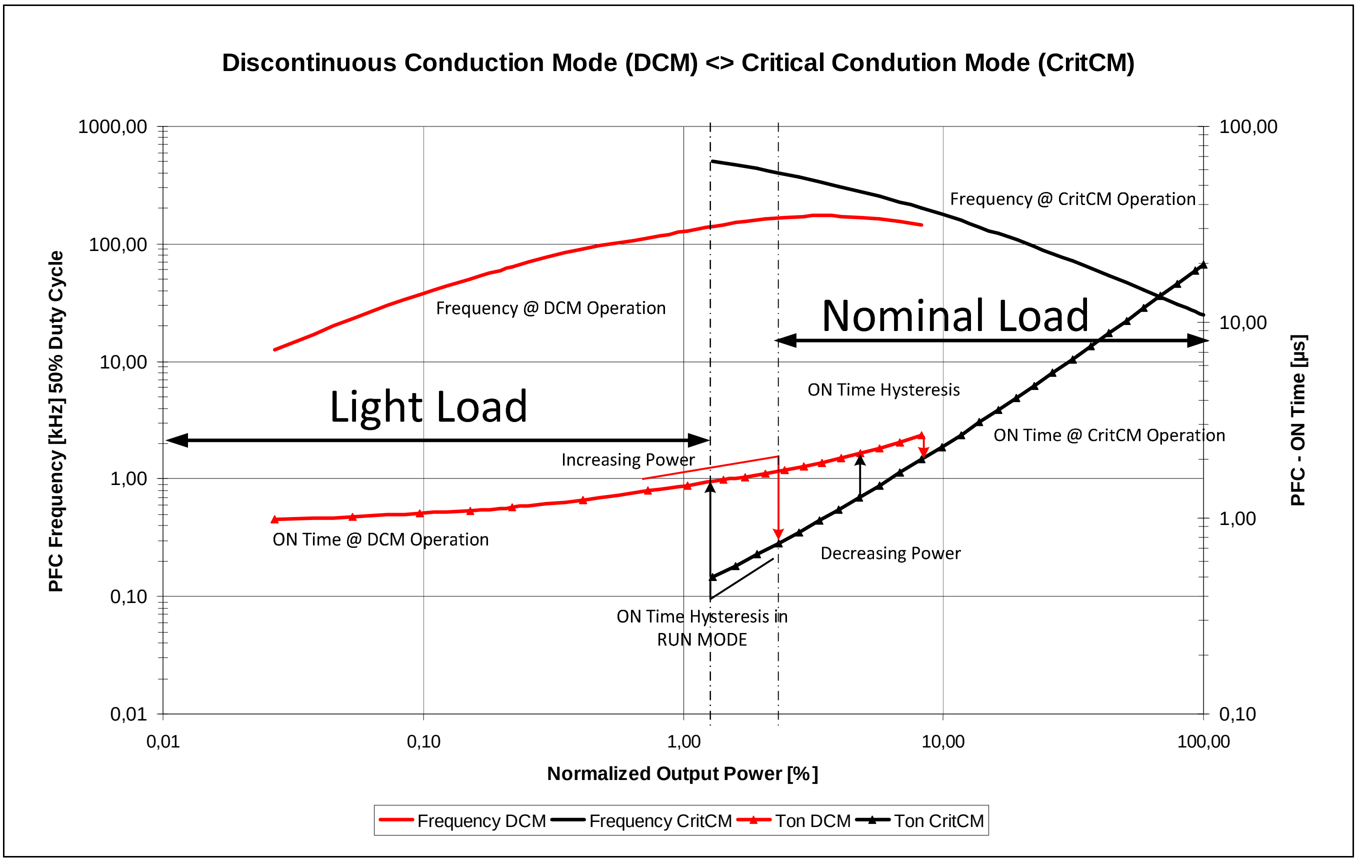


Figure 12 PFC DCM / CritCM vs Power and ON Time

For lower loads ($P_{OUTNorm}$ < 8 % of the normalized load[1]) the controller operates in discontinuous conduction mode (DCM) with an ON time of 4.0 µs and increasing OFF time. The frequency during DCM is variable in a range from 144 kHz down to typically 22 kHz @ 0.1 % load. With this control method, the PFC converter enables stable operation from a 100 % load down to 0.1 %. Figure 12 PFC DCM / CritCM vs Power and ON Time) shows the ON time range in DCM and CritCM (Critical Conduction Mode) operation. In the overlapping area of CritCM and DCM there is a hysteresis of the ON time, which causes a negligible frequency change.

[1] Normalized Power @ Low Line Input Voltage and maximum Lload

2.3.2 PFC Bus Overvoltage and Open Loop

The bus voltage loop control is completely integrated (Figure 13 PFC Bus Voltage Operating and Error Levels) and provided by an 8-bit sigma-delta A/D converter with a typical sampling rate of 280 µs and a resolution of 4 mV/bit. After leaving monitoring, the IC starts to power up (VCC > 14.0 V). After power-up, the IC senses the bus voltage below 12.5 % (open loop) or above 105 % (bus overvoltage) for 80 µs – 130 µs. In the case of bus overvoltage ($V_{BUSrated}$ > 109 %) or open loop ($V_{BUSrated}$ < 12.5 %), the IC shuts off the gate drives of the PFC within 5 µs or 1 µs respectively. In this case, the PFC restarts automatically when the bus voltage is within the corridor (12.5 % < $V_{BUSrated}$ < 105 %) again. If the bus voltage is valid after the 130 µs, the bus voltage sensing is set to 12.5 % < $V_{BUSrated}$ < 109 %. If these thresholds are departed from for longer than 1 µs (open loop) or 5 µs (overvoltage), the PFC gate drive stops working until the voltage drops below 105 % or exceeds the 12.5 % level. If the bus overvoltage (> 109 %) lasts for longer than 625 ms in run mode, the inverter gates also shut off and a power-down with complete restart is attempted (Figure 13 PFC Bus Voltage Operating and Error Levels).

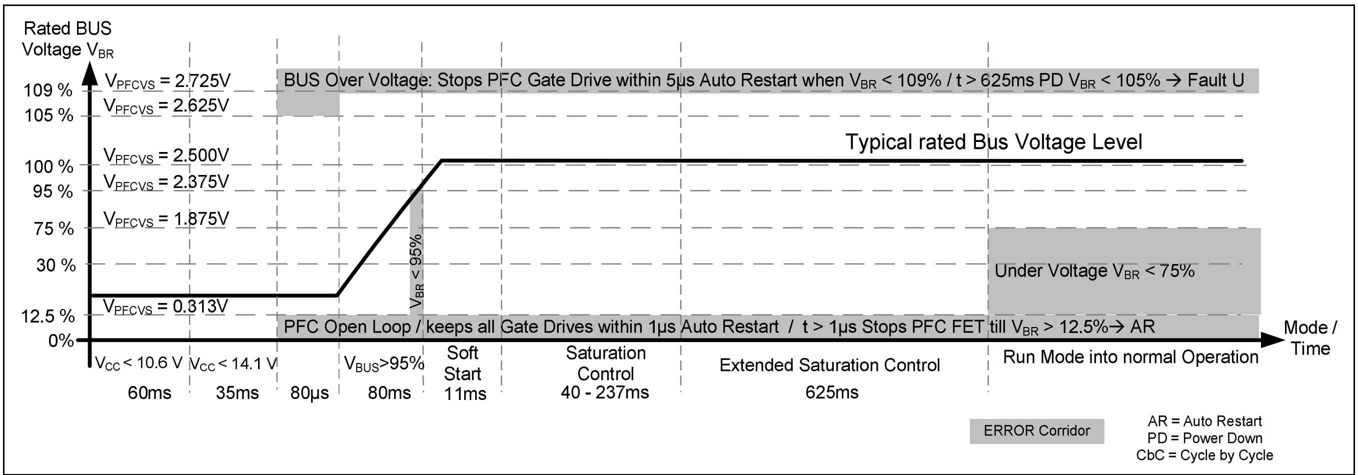


Figure 13 PFC Bus Voltage Operating and Error Levels

2.3.3 PFC Bus Voltage Levels 95 % and 75 %

When the rated bus voltage is in the corridor of 12.5 % < $V_{BUSrated}$ < 109 %, the IC will check whether the bus voltage exceeds the 95 % threshold (Figure 13 PFC Bus Voltage Operating and Error Levels) within 80 ms before entering soft start phase. Another threshold is activated when the IC enters the run mode. If the rated bus voltage drops below 75 % for longer than 84 µs, a power-down with a complete restart is attempted if a counter exceeds 800 ms. In the case of short-term bus undervoltage (the bus voltage reaches its working level in run mode before exceeding typically 800 ms - min. 500 ms) the IC skips phases and starts up directly in saturation control. The internal reference level of the bus voltage sense V_{PFCVS} is 2.5 V (100 % of the rated bus voltage) with a high accuracy. Surge protection is activated in the case of a rated bus voltage of V_{BUS} > 109 % and a low-side current sense voltage of V_{LSCS} > 1.6 V in extended saturation mode or of V_{LSCS} > 0.8 V in run mode for longer than 500 ns in extended saturation mode.

2.3.4 PFC Structure of Mixed Signals

A digital NOTCH filter eliminates the input voltage ripple independent of the mains frequency. A subsequent error amplifier with PI characteristic ensures stable operation of the PFC preconverter (Figure 14 PFC Mixed Signal Structure).

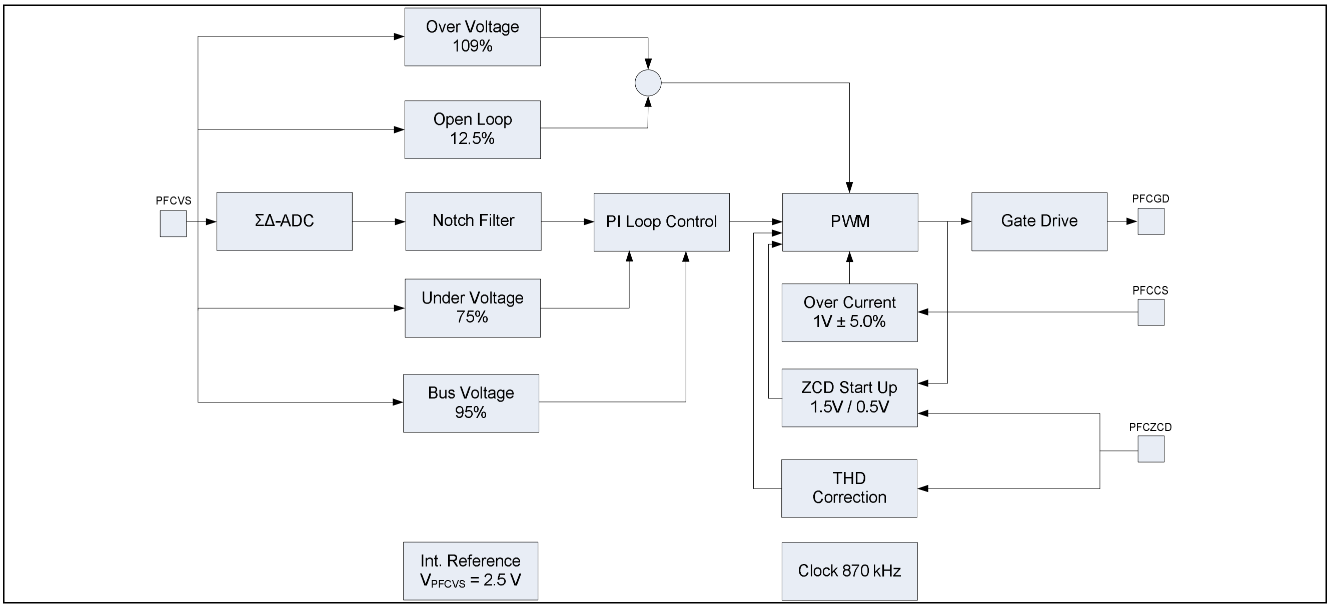


Figure 14 PFC Mixed Signal Structure

The zero current detection (ZCD) is sensed by the PFC ZCD. Indication of finished current flow during demagnetization is required in CritCM and in DCM as well. The input is equipped with a special filtering, including an extended saturation of typically 500 ns and a large hysteresis of typically 0.5 V and 1.5 V V_{PFCZCD}.

2.3.5 THD Correction via Zero Crossing Detection Singal

An additional feature is the THD correction (Figure 15 THD Improvement – Automatic Pulse Width). In order to optimize the improved THD (especially in the zones A shown in , ZCD @ AC input voltage), there is a possibility to extend the pulse width of the gate signal (blue part of the PFC gate signal) via the variable PFC ZCD resistor from the ZCD pin to the PFC choke in addition to the gate signal controlled by the V_{PFCVS} signal (gray part of the PFC gate signal).

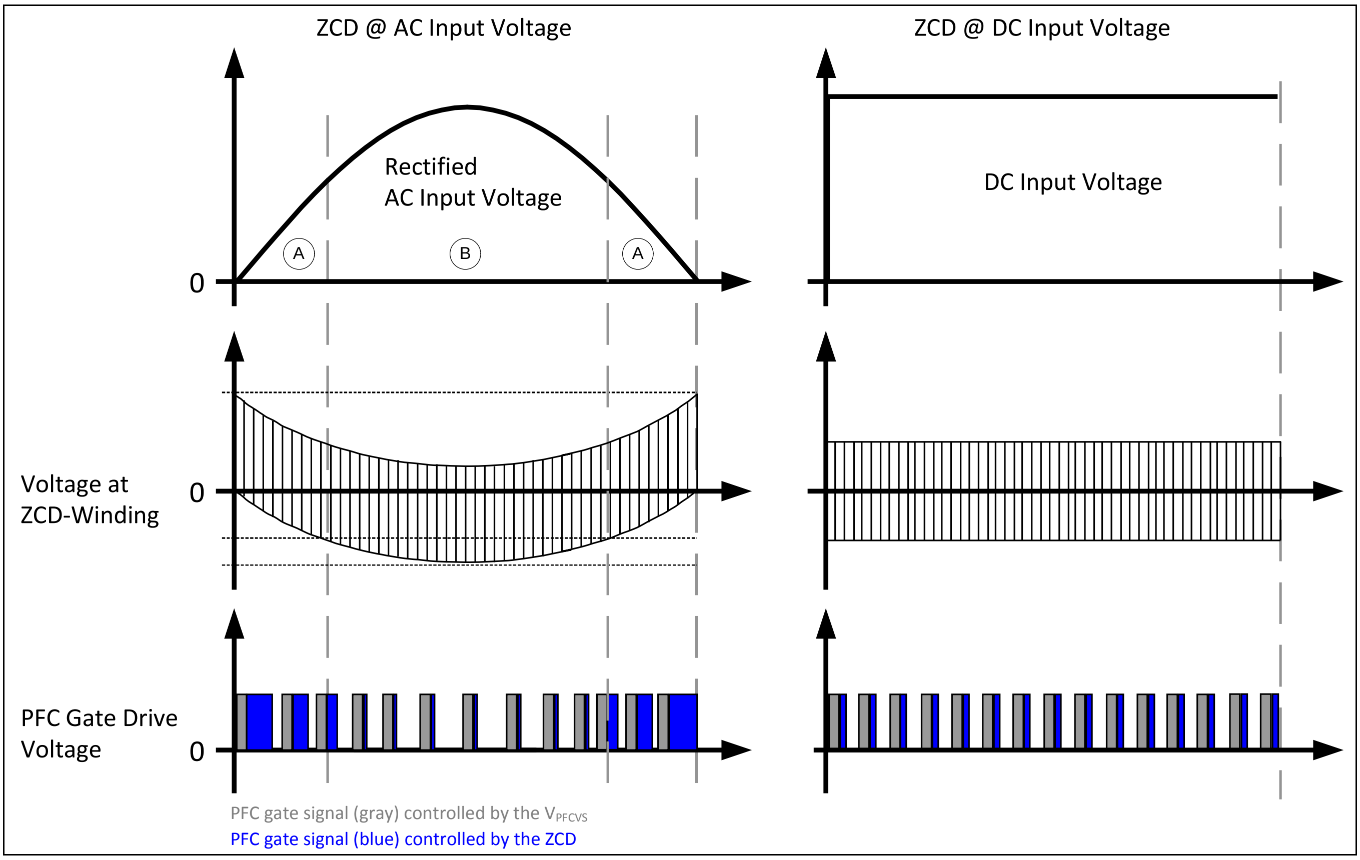


Figure 15 THD Improvement – Automatic Pulse Width Extension

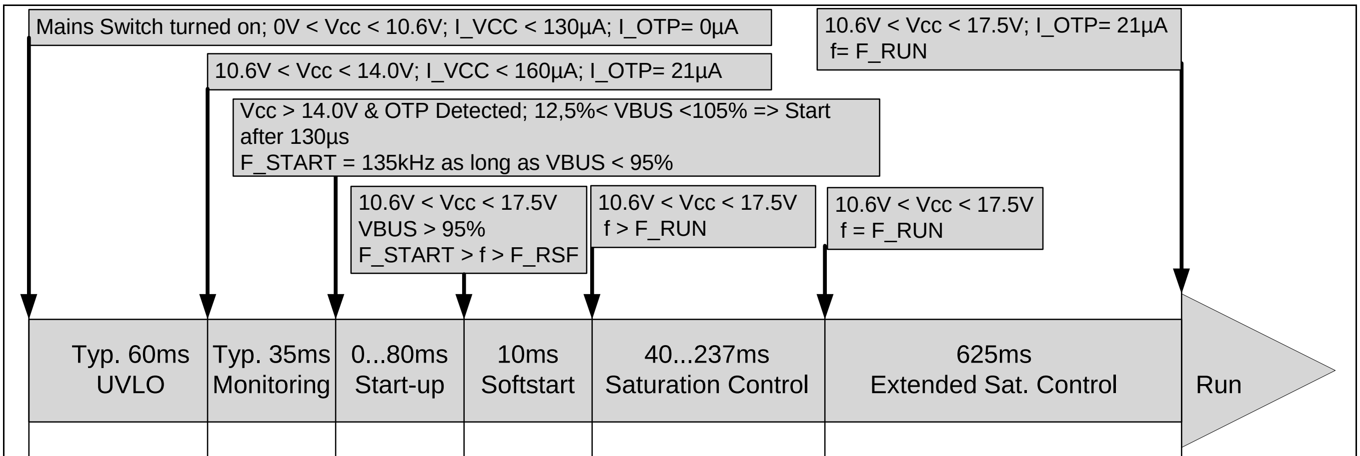
In the case of DC input voltage, the pulse width gate signal is fixed as a combination of the gate signal controlled by the V_{PFCVS} pin (gray) and the additional pulse width signal controlled by the ZCD pin (blue) ZCD @ DC input voltage.
The PFC current limitation at pin PFCCS interrupts the ON time of the PFC MOSFET if the voltage drop at the PFC shunt resistors exceeds V_{PFCCS} = 1.0 V. This interrupt will restart after the next sufficient signal from ZCD becomes available (auto restart). The first value of the resistor can be calculated as the ratio of the PFC mains choke and ZCD winding times the bus voltage to a current of typically 1.5 mA (see equation below). An adjustment of the ZCD resistor causes an optimized THD.

$$R_{ZCD} = \frac{\frac{N_{ZCD}}{N_{PFC}} * V_{BUS}}{1.5mA}$$

Equation 1: R_{ZCD} – A Good Practical Value

2.4 State Diagram

2.4.1 Monitoring of Features versus Operating Mode



Feature	Type	0...80ms Start-up	10ms Softstart	40...237ms Saturation Control	625ms Extended Sat. Control		Run
BUS Overvoltage > 109%	U	enabled PFC	enabled PFC	enabled PFC	enabled PFC	enabled PFC	enabled PFC 5µs enabled Inv 625ms
BUS Overvoltage > 105%	A	enabled 130µs					
BUS Undervoltage < 95%	A	enabled					
BUS Undervoltage < 75%	U						enabled 84µs
BUS Open Loop < 12,5%	U	enabled PFC	enabled PFC	enabled PFC	enabled PFC	enabled PFC	enabled PFC 5µs enabled Inv 625ms
Overcurrent PFC	A	enabled	enabled	enabled	enabled	enabled	enabled 200ns Threshold 1.0V
Overcurrent Inverter	F	enabled 1,6V	enabled 1,6V	enabled 0,8V	enabled 1,6V	enabled 1,6V	enabled 500ns Threshold 0.8V
Capacitive Load	F						enabled 620µs
OVP, Overload	F						enabled 620µs

A = Auto Restart / F = Fault, checked with a single Restart / U = UVLO

Figure 16 Monitoring of Features versus Operation Mode

2.4.2 Fault Condition – Flow Chart Fault F Latch OFF / Single Restart / Restart

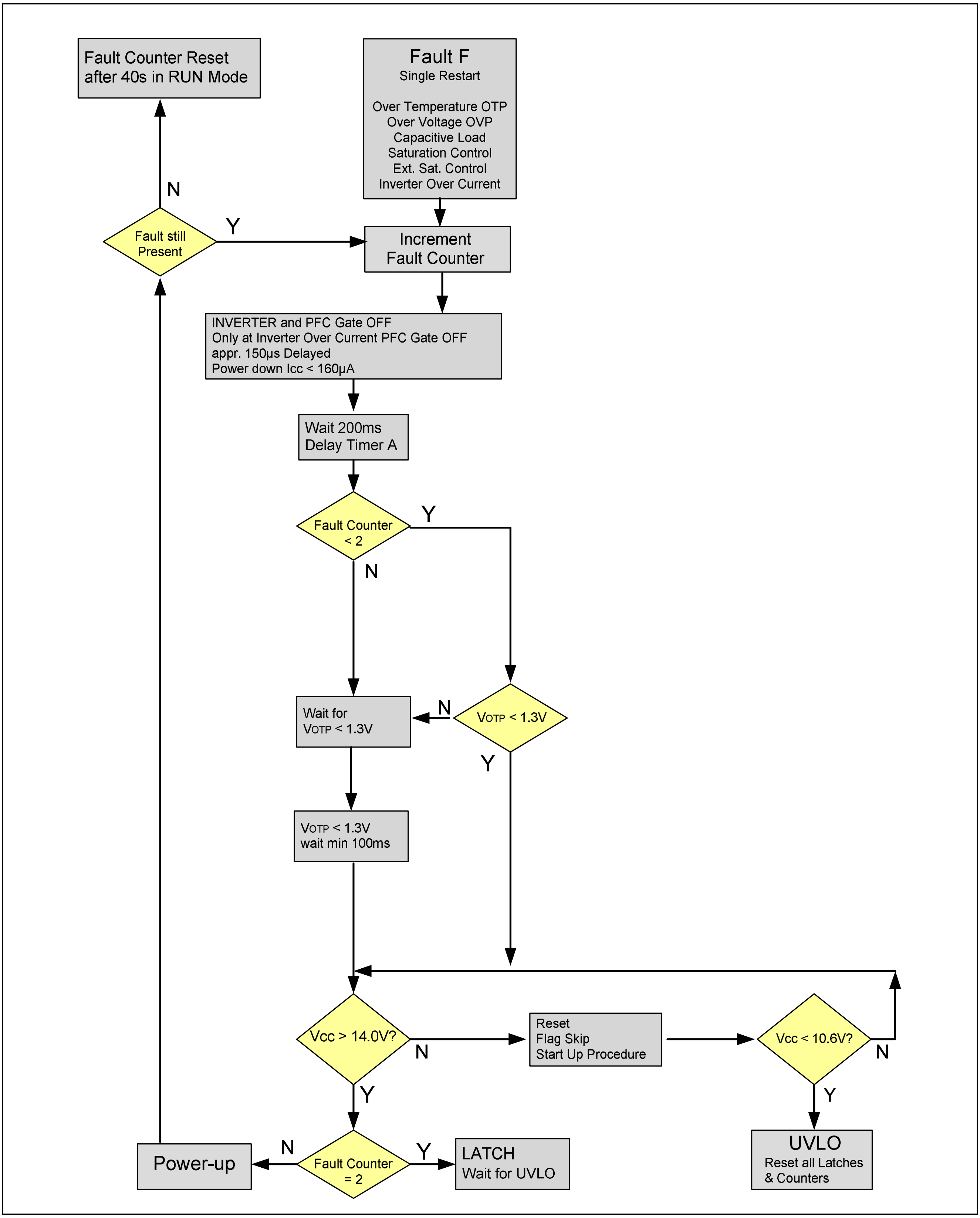


Figure 17 Fault Condition – Flow Chart Latch OFF / Single Restart / Restart

2.4.3 Fault Condition – Flow Chart Fault A Auto Restart

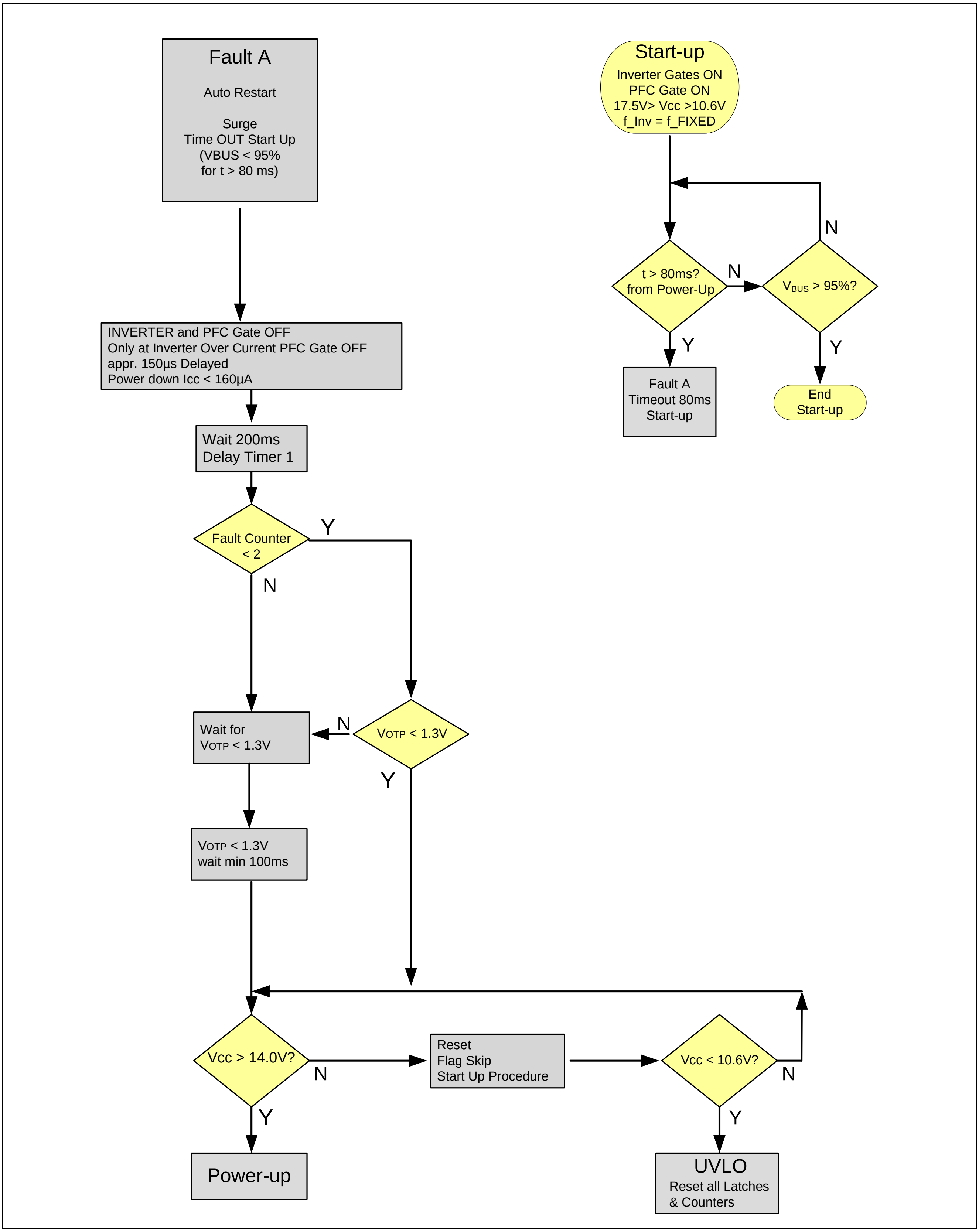


Figure 18 Fault Condition – Auto Restart

2.4.4 Fault Condition – Flow Chart Fault U BUS Voltage

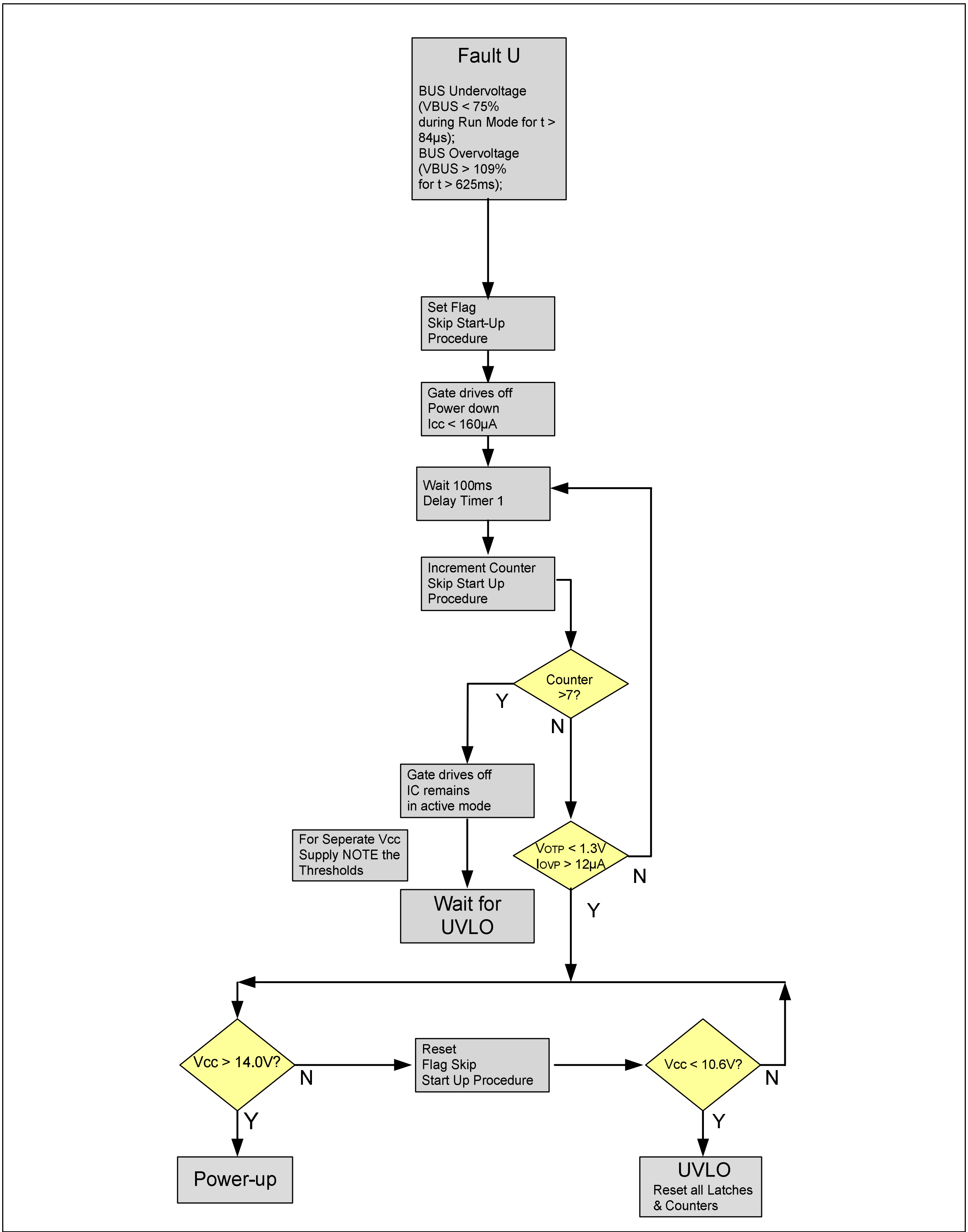


Figure 19 Fault Condition – Auto Restart

2.4.5 Protection Matrix

Description of Fault	Characteristics of Fault			Operating Mode Detection is active							Consequence
	Name of fault	Type of fault	Minimum duration of effect	Monitoring	Power-up 130µs	Start-up until VBUS > 95%	Softstart 10ms	Saturation control 40 ms typ.	Ext. Sat. Con. 625ms	Run mode	
Supply voltage Vcc < 14.1V before power up	Below start-up threshold	S	1µs	X							Prevents power up
Supply voltage Vcc < 10.6V after power up	Below UVLO threshold	S	5µs	X	X	X	X	X	X	X	Power down, Reset failure latch
Voltage at OTP pin > 1.6V before power up	Overtemperature	S	100µs	X							Prevents power up
Voltage at OTP pin > 3.2V	Overtemperature	F	620µs							X	Power down, latched fault mode, 1 restart
Bus voltage < 12.5% of rated level 10µs after power up	Open loop detection	S	1µs		X						Keep gate drives off, re-start after Vcc hysteresis
Bus voltage < 12.5% of rated level	Open loop detection	N	1µs			X	X	X	X	X	Stops PFC FET until VBUS > 12.5%
Bus voltage < 12.5% of rated level	Shutdown option	U	625ms							X	Power down, restart when VBUS> 12.5%
Bus voltage < 75% of rated level add. shut down delay 120µs	Undervoltage	U	84µs							X	Power down, 100ms delay, restart directly with saturation control
Bus voltage < 95% of rated level during start-up	Timeout max start-up time	A	80ms			X					Power down, 200ms delay, restart
Bus voltage > 105% of rated level 10µs after power up	PFC overvoltage	S	5µs		X						Keep gate drives off, re-start after Vcc hysteresis
Bus voltage > 109% of rated level in active operation	PFC overvoltage	N	5µs			X	X	X	X	X	Stops PFC FET until VBUS< 105%
Bus voltage > 109% of rated level in active operation	Inverter overvoltage	U	625ms							X	Power down, restart when VBUS<105%
peak level of output voltage at Pin OVP above threshold	Output overvoltage	F	620µs							X	Power down, latched fault mode, 1 restart
Capacitive Load operation below resonance	Overload	F	620µs							X	Power down, latched fault mode, 1 restart
Voltage at PFCCS pin > 1.0V	PFC overcurrent	N	200ns			X	X	X	X	X	Stops on-time of PFC FET immediately
Voltage at LSCS pin > 0.8V	Inverter current lim	N	200ns					X			Activates saturation control
Voltage at LSCS pin > 1.2V & 205mV/µs Slope in 0.8V	Saturation Time OUT	F	237ms					X			Power down, latched fault mode, 1 restart
Voltage at LSCS pin > 0.8V & 205mV/µs Slope	Ext. Sat. Time OUT	F	625ms						X		Power down, latched fault mode, 1 restart
Voltage at LSCS pin > 0.8V	Inverter overcurrent	F	500ns							X	Power down, latched fault mode, 1 restart
Voltage at LSCS pin > 1.6V	Inverter overcurrent	F	500ns			X	X	X	X		Power down, latched fault mode, 1 restart
Voltage at LSCS pin > 0.8V & VBUS > 109% (Surge)	Inverter overcurrent	A	500ns						X	X	Power down, restart when VBUS<109%
After jump into latched fault mode F wait			200ms	A single restart attempt after delay of internal timer							
Reset of failure latch in run mode after			40s	Reset of failure latch by UVLO or 40s in run mode							
S = Start-up condition, N = No fault, A = Auto restart , U = Undervoltage											
F = Fault with a single restart, a second F leads to a latched fault / **Note: all values @ typical 50 Hz mains frequency**											

3 Electrical Characteristics

Note: All voltages without the high-side signals are measured with respect to ground (pin 4). The high-side voltages are measured with respect to pin 17. The voltage levels are valid if other ratings are not violated.

3.1 Absolute Maximum Ratings

Note: Absolute maximum ratings are defined as ratings, which if exceeded may lead to destruction of the integrated circuit. For the same reason make sure that any capacitor connected to pin 3 (VCC) and pin 18 (HSVCC) is discharged before assembling the application circuit.

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
LSCS Voltage	V_{LSCS}	- 5	6	V	
LSCS Current	I_{LSCS}	- 3	3	mA	
LSGD Voltage	V_{LSGD}	- 0.3	V_{cc}+0.3	V	Internally clamped to 11V
LSGD Peak Source Current	$I_{LSGDsomax}$	- 75	5	mA	< 500 ns
LSGD Peak Sink Current	$I_{LSGDsimax}$	- 50	400	mA	< 100 ns
VCC Voltage	V_{VCC}	- 0.3	18.0	V	
VCC Zener Clamp Current	$I_{VCCzener}$	- 5	5	mA	IC in Power Down Mode
PFCGD Voltage	V_{PFCGD}	- 0.3	V_{cc}+0.3	V	
PFCGD Peak Source Current	$I_{PFCGDsomax}$	- 150	5	mA	< 500 ns
PFCGD Peak Sink Current	$I_{PFCGDsimax}$	- 100	700	mA	< 100 ns
PFCCS Voltage	V_{PFCCS}	- 5	6	V	
PFCCS Current	I_{PFCCS}	- 3	3	mA	
PFCZCD Voltage	V_{PFCZCD}	- 3	6	V	
PFCZCD Current	I_{PFCZCD}	- 5	5	mA	
PFCVS Voltage	V_{PFCVS}	- 0.3	5.3	V	
RFM Voltage	V_{RFM}	- 0.3	5.3	V	
OTP Voltage	V_{OTP}	- 0.3	5.3	V	
OVP Voltage	V_{OVP}	- 6	7	V	
OVP Current1	I_{OVP_1}	- 1	1	mA	IC in Power Down Mode
OVP Current2	I_{OVP_2}	- 3	3	mA	IC in active mode
HSGND Voltage	V_{HSGND}	- 650	650	V	Referring to GND 1)
HSGND Voltage Transient	dV_{HSGND}/dt	- 40	40	V/ns	
HSVCC Voltage	V_{HSVCC}	- 0.3	18.0	V	Referring to HSGND

1) Limitation due to voltage capability in end test

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
HSGD Voltage	V_{HSGD}	- 0.3	V_{HSVCC}+0.3	V	Internally clamped to 11V
HSGD Peak Source Current	$I_{HSGDsomax}$	- 75	0	mA	< 500ns
HSGD Peak Sink Current	$I_{HSGDsimax}$	0	400	mA	< 100ns
Junction Temperature	T_J	- 40	150	°C	
Storage Temperature	T_S	- 55	150	°C	
Maximum Power Dissipation	P_{TOT}	—	1	W	PG_DSO-16 / T_{amb}=25°C
Thermal Resistance (2 Chips) Junction - Ambient	R_{thJA}	—	125	K/W	PG_DSO-16 @ TA = 85°C & PCB Area > 30x20mm
Soldering Temperature Wave		—	260	°C	Wave Soldering[1)]
Soldering Temperature Reflow		—	[2)]	°C	Reflow Soldering
ESD Capability HBM	V_{ESD_HBM}	—	2	kV	Human Body Model[3)]
ESD Capability CDM	V_{ESD_CDM}	—	1	kV	Charged Device Model[4)]
Rated Bus Voltage (95%)	$V_{PFCVS95}$	2.33	2.43	V	

1) According to JESD22A111
2) According to J-STD-020D
3) According to EIA/JESD22-A114-B
4) According to JESD22-C101

3.2 Operating Range

The IC operates as described in the functional description once the values listed here lie within the operating range.

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	Max.		
HSVCC Supply Voltage	V_{HSVCC}	$V_{HSVCCOff}$	17.5	V	Referring to HSGND
HSGND Voltage	V_{HSGND}	- 650	650	V	Referring to GND[1]
VCC Voltage @ 25°C	V_{VCC}	V_{VCCOff}	17.5	V	T_J = 25°C
VCC Voltage @ 125°C	V_{VCC}	V_{VCCOff}	18.0	V	T_J = 125°C
LSCS Voltage Range	V_{LSCS}	- 4	5	V	In active mode
PFCVS Voltage Range	V_{PFCVS}	0	4	V	
PFCCS Voltage Range	V_{PFCCS}	- 4	5	V	In active mode
PFZCD Current Range	I_{PFCZCD}	- 3	3	mA	In active mode
OVP Voltage Range	V_{OVP}	- 6	6 [2]	V	
OVP, Current Range	I_{OVP}	[3]	210	µA	IC Power Down Mode
OVP, Current Range	I_{OVP}	- 2.5	2.5	mA	IC active mode
Junction Temperature	T_j	- 40	125	°C	
Adjustable Run Frequency	f_{RFM}	20	120	kHz	Range set by RFM
Adjustable Run Frequency	f_{RFM}	20	130	kHz	@ - 25°C
Set Resistor for Run Freq.	R_{RFM}	4.1	25	kΩ	
Mains Frequency	f_{Mains}	45	65	Hz	NOTCH Filter Operation

[1] Limitation due to creeping distance between the HS & LS Pins (CTT 900V inside)
[2] Limited by maximum of current range at OVP
[3] Limited by minimum of voltage range at OVP

3.3 Characteristics Power Supply Section

Note: The electrical characteristics involve the spread of values given within the specified supply voltage and junction temperature range T_J from -40 °C to 125 °C. Typical values represent the median values, which are given in reference to 25 °C. If not otherwise stated, a supply voltage of 15 V and V_{HSVCC} = 15 V is assumed and the IC operates in active mode. Furthermore, all voltages refer to GND if not otherwise mentioned.

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
VCC Quiescent Current1	I_{VCCqu1}	—	90	130	µA	$V_{VCC} = V_{VCCOff} - 0.5V$
VCC Quiescent Current2	I_{VCCqu2}	—	120	160	µA	$V_{VCC} = V_{VCCOn} - 0.5V$
VCC Supply Current [1]	$I_{VCCSupply}$	—	4.2	6.0	mA	$V_{PFCVS} > 2.725V$
VCC Supply Current in Latched Fault Mode	$I_{VCCLatch}$	—	110	170	µA	V_{OTP} = 5V
LSVCC Turn-On Threshold LSVCC Turn-Off Threshold LSVCC Turn-On/Off Hyst.	V_{VCCOn} V_{VCCOff} V_{VCCHys}	13.48 10.0 3.2	14.0 10.6 3.6	14.5 11.0 4.0	V V V	 Hysteresis
VCC Zener Clamp Voltage	$V_{VCCClamp}$	15.5	16.3	16.9	V	I_{VCC} = 2mA/V_{OTP} = 5V
VCC Zener Clamp Current	$I_{VCCZener}$	2.5	—	5.05	mA	V_{VCC} = 17.5V/V_{OTP} = 5V
High Side Leakage Current	$I_{HSGNDleak}$	—	0.01	2	µA	V_{HSGND} = 650V, V_{GND}=0V
HSVCC Quiescent Current	$I_{HSVCCqu1}$[2]	—	190	280	µA	$V_{HSVCC} = V_{HSVCCOn} - 0.5V$
HSVCC Quiescent Current[1]	$I_{HSVCCqu2}$[2]	0.26	0.65	1.2	mA	$V_{HSVCC} > V_{HSVCCOn}$
HSVCC Turn-On Threshold HSVCC Turn-Off Threshold HSVCC Turn-On/Off Hyst.	$V_{HSVCCOn}$[2] $V_{HSVCCOff}$[2] $V_{HSVCCHy}$[2]	9.75 8.08 1.4	10.4 8.6 1.7	11.0 9.3 2.03	V V V	Hysteresis
Low Side Ground	GND					

[1] With inactive gate
[2] Refers to high-side ground (HSGND)

3.4 Characteristics of PFC Section

3.4.1 PFC Current Sense (PFCCS)

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Turn-off threshold	$V_{PFCCSOff}$	0.95	1.0	1.05	V	
Overcurrent blanking + propagation delay[1]	$t_{PFCCSOff}$	140	200	262	ns	
Leading-edge blanking	$t_{Blanking}$	180	250	315	ns	Pulse width when V_{PFCCS} > 1.0V
PFCCS bias current	$I_{PFCCSBias}$	- 0.5	—	0.5	µA	V_{PFCCS} = 1.5V

[1] Propagation Delay = 50 ns

3.4.2 PFC Zero Current Detection (PFCZCD)

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Zero crossing upper thr. [1]	$V_{PFCZCDUp}$	1.4	1.5	1.6	V	
Zero crossing lower thr. [2]	$V_{PFCZCDLow}$	0.4	0.5	0.6	V	
Zero crossing hysteresis	$V_{PFCZCDHys}$	—	1.0	—	V	
Clamping of pos. voltages	$V_{PFCZCDpclp}$	4.1	4.6	5.12	V	$I_{PFCZCDSink}$ = 2mA
Clamping of neg. voltages	$V_{PFCZCDnclp}$	- 1.69	- 1.4	- 1.0	V	$I_{PFCZCDSource}$ = - 2mA
PFCZCD bias current	$I_{PFCZCDBias}$	- 0.5	—	5.0	µA	V_{PFCZCD} = 1.5V
PFCZCD bias current	$I_{PFCZCDBias}$	- 0.5	—	0.5	µA	V_{PFCZCD} = 0.5V
PFCZCD ringing su.[3] time	$t_{Ringsup}$	350	500	660	ns	
Limit value for ON time extension	$\Delta t \times I_{ZCD}$	498	700	900	pAxs	

1) Turn-OFF threshold
2) Turn-ON threshold
3) Ringing suppression time

3.4.3 PFC Voltage Sensing Bus (PFCVS)

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	Typ.	max.		
Trimmed reference voltage	$V_{PFCVSRef}$	2.468	2.50	2.53	V	
Overvoltage turn-off (109 %)	$V_{PFCVSRUp}$	2.677	2.73	2.78	V	
Overvoltage turn-on (105 %)	$V_{PFCVSLow}$	2.567	2.63	2.68	V	
Overvoltage hysteresis	$V_{PFCVSHys}$	70	100	130	mV	4 % rated bus voltage
Undervoltage (75 %)	$V_{PFCVSUV}$	1.832	1.88	1.915	V	
Undervoltage (12.5 %)	$V_{PFCVSUV}$	0.237	0.31	0.387	V	
Rated bus voltage (95 %)	$V_{PFCVS95}$	2.320	2.38	2.425	V	
PFCVS bias current	$I_{PFCVSBias}$	- 1.0	—	1.0	µA	V_{PFCVS} = 2.5V

3.4.4 PFC PWM Generation

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	Typ.	max.		
Initial ON time [1]	$t_{PFCON\_initial}$	—	4.0	—	µs	V_{PFCZCD} = 0V
Max. ON time [2]	t_{PFCON_max}	18.0	24.0	28.6	µs	0.45V < V_{PFCVS} < 2.45V
Switch threshold from CritCM to DCM	t_{PFCON_min}	160	270	370	ns	
Repetition time [1]	t_{PFCRep}	47	52	57	µs	V_{PFCZCD} = 0V
Off time	t_{PFCOff}	42	47	52.5	µs	

1) When missing zero crossing signal
2) At the maximum of the AC line input voltage

3.4.5 PFC Gate Drive (PFCGD)

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	Typ.	max.		
PFCGD Low Voltage	$V_{PFCGDLow}$	0.4	0.7	0.92	V	I_{PFCGD} = 5mA
		0.4	0.75	1.12	V	I_{PFCGD} = 20mA
		- 0.2	0.3	0.62	V	I_{PFCGD} = -20mA
PFCGD High Voltage	$V_{PFCGDHigh}$	10.0	11.0	11.6	V	I_{PFCGD} = -20mA
		8.98	—	—	V	I_{PFCGD} = -1mA / V_{VCC} 1)
		8.47	—	—	V	I_{PFCGD} = -5mA / V_{VCC} 1)
PFCGD active Shut Down	$V_{PFCGASD}$	0.4	0.75	1.12	V	I_{PFCGD} = 20mA V_{VCC}=5V
PFCGD UVLO Shut Down	$V_{PFCGDuvlo}$	0.3	1.0	1.56	V	I_{PFCGD} = 5mA V_{VCC}=2V
PFCGD Peak Source Current	$I_{PFCGDSouce}$	—	- 100	—	mA	2) + 3)
PFCGD Peak Sink Current	$I_{PFCGDSink}$	—	500	—	mA	2) + 3)
PFCGD Voltage during sink Current	$V_{PFCGDHigh}$	11.0	11.7	12.3	V	$I_{PFCGDSinkH}$ = 3mA
PFC Rise Time	$t_{PFCGDRise}$	80	245	500	ns	2V > VLSGD > 8V 2)
PFC Fall Time	$t_{PFCGDFall}$	20	45	72	ns	8V > VLSGD > 2V 2)

1) $V_{VCC} = V_{VCCOff} + 0.3V$
2) $R_{Load} = 4\Omega$ and $C_{Load} = 3.3nF$
3) The parameter is not subject to production testing – verified by design/characterization

3.5 Characteristics of Inverter Section

3.5.1 Low-Side Current Sense (LSCS)

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Overcurrent shutdown volt.	$V_{LSCSOvC1}$	1.5	1.6	1.7	V	1)
Overcurrent shutdown Volt.	$V_{LSCSOvC2}$	0.75	0.8	0.85	V	2)
Duration of overcurrent	$t_{LSCSOvC}$	450	600	700	ns	
Capacitive mode det. Level1	$V_{LSCSCap1}$	- 70	- 50	- 27	mV	
Capacitive mode duration1	$t_{LSCSCap1}$	—	280	—	ns	3)
Capacitive mode det. Level2	$V_{LSCSCap2}$	1.8	2.0	2.2	V	During RUN Mode
Capacitive mode duration2	$t_{LSCSCap2}$	—	50	—	ns	4)
LSCS bias current	$I_{LSCSBias}$	-1.0	—	1.0	µA	@ V_{LSCS} = 1.5 V

1) Overcurrent voltage threshold active during start-up, soft start, saturation control and extended saturation mode
2) Overcurrent voltage threshold active during run mode
3) Active before turn-ON of the HSGD in run mode
4) Active during turn-ON of the HSGD in run mode

3.5.2 Low-Side Gate Drive (LSGD)

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
LSGD low voltage	$V_{LSGDLow}$	0.4	0.7	1.02	V	I_{LSGD} = 5 mA [1]
		0.4	0.8	1.22	V	I_{LSGD} = 20 mA [1]
		- 0.3	0.2	0.53	V	I_{LSGD} = - 20 mA (source)
LSGD high voltage	$V_{LSGDHigh}$	10.0	10.8	11.6	V	[2]
		8.98	—	—	V	[3]
		8.47	—	—	V	[4]
LSGD active shutdown	$V_{LSGDASD}$	0.4	0.75	1.12	V	V_{CC} = 5 V / I_{LSGD} = 20 mA [1]
LSGD UVLO shutdown	$V_{LSGDUVLO}$	0.3	1.0	1.6	V	V_{CC} = 2 V / I_{LSGD} = 5 mA [1]
LSGD peak source current	$I_{LSGDSource}$	—	- 50	—	mA	[5) + 6)]
LSGD peak sink current	$I_{LSGDSink}$	—	300	—	mA	[5) + 6)]
LSGD voltage during [1]	$V_{LSGDHigh}$	—	11.7	—	V	$I_{LSGDsinkH}$ = 3 mA
LSGD rise time	$t_{LSGDRise}$	80	245	500	ns	2 V < V_{LSGD} < 8 V [5]
LSGD fall time	$t_{LSGDFall}$	20	35	61	ns	8 V > V_{LSGD} > 2 V [5]

1) Sink current
2) I_{LSGD} = –20 mA source current
3) V_{CCOFF} + 0.3 V and I_{LSGD} = –1 mA source current
4) V_{CCOFF} + 0.3 V and I_{LSGD} = –5 mA source current
5) Load: R_{Load} = 10 Ω and C_{Load} = 1 nF
6) The parameter is not subject to production testing – verified by design/characterization

3.5.3 Inverter Minimum Run Frequency (RFM)

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Fixed start-upfrequency	$f_{StartUp}$	120	135	148.5	kHz	
Duration of soft start	$t_{SoftStart}$	9	11	13.56	ms	[1]
RFM voltage in run mode	V_{RFM}	—	2.5	—	V	@ 100µA<I_{RFM}<600µA
Run frequency	f_{RFM}	49	50	51.1	kHz	R_{RFM} = 10kΩ [2]
Adjustable run frequency	f_{RFM1}	—	20	—	kHz	I_{RFM}= - 100 µA [2]
	f_{RFM2}	—	40	—	kHz	I_{RFM}= - 200 µA [2]
	f_{RFM3}	—	100	—	kHz	I_{RFM}= - 500 µA [2]
	f_{RFM4}	—	120	—	kHz	I_{RFM}= - 600 µA [2]
	$f_{RFM-25°C}$	—	130	—	kHz	I_{RFM}= - 650 µA [3]
RFM max. current range	I_{RFMmax}	—	-1000	- 612	µA	@ VRFM = 0V [2]

1) Shift start-up frequency to run frequency
2) Run frequency @ - 40°C
3) Run frequency @ - 25°C

3.5.4 Overtemperature Protection (OTP)

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Over Temperature Detection	V_{OTP1}	1.546	1.60	1.65	V	UVLO, $V_{CC} < V_{CCON}$
	V_{OTP2}	1.247	1.30	1.35	V	
	V_{OTP3}	—	3.2	—	V	Run Mode
OTP Current Source	I_{OTP1}	- 53.2	-42.6	-30.5	µA	V_{OTP} = 1V ; OVP = 5µA
	I_{OTP2}	-44.2	-35.4	-25.1	µA	V_{OTP} = 2V ; OVP = 5µA
	I_{OTP3}	- 26.6	-21.3	- 15.0	µA	V_{OTP} = 1V ; OVP = 30µA
	I_{OTP4}	- 22.1	-17.7	-12.3	µA	V_{OTP} = 2V ; OVP = 30µA

3.5.5 Overvoltage Protection (OVP)

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Source Current before Start-Up	$I_{OVPSource}$	- 5.0	- 3.0	- 1.9	µA	V_{OVP} = 0V
Enable Monitoring	$V_{OVPEnable1}$	350	530	750	mV	1)
Sink Current for OVP	$I_{OVPSink}$	7.0	12.0	18.0	µA	
Positive Clamping Voltage	$V_{OVPClamp}$	—	6.5	—	V	@ I_{OVP} = 300µA
AC OVP Current Threshold	$I_{OVPSource}$	186	210	230	µApp	
Positive OVP Current Thr.	$I_{OVPDCPos}$	34	42	50	µApp	
Neative OVP Current Thr.	$I_{OVPDCNeg}$	- 50	- 42	- 34	µApp	

1) If $V_{OTP} < V_{OTPEnable1}$ monitoring is disabled

3.5.6 High Side Gate Drive (HSGD)

Parameter	Symbol	Limit Values			Unit	Test Condition
		Min.	typ.	max.		
HSGD Low Voltage	$V_{HSGDLow}$	0.018	0.05	0.1	V	I_{HSGD} = 5mA (sink)
		0.46	1.1	2.5	V	I_{HSGD} = 100mA (sink)
		- 0.4	- 0.2	- 0.04	V	I_{LSGD} = - 20mA (source)
HSGD High Voltage	$V_{HSGDHigh}$	9.7	10.5	11.2	V	V_{CCHS}=15V I_{HSGD} = - 20mA (source)
		7.8	—	—	V	$V_{CCHSOFF}$ + 0.3V I_{HSGD} = - 1mA (source)
HSGD active Shut Down	$V_{HSGDASD}$	0.041	0.22	0.5	V	V_{CCHS}=5V I_{HSGD} = 20mA (sink)
HSGD Peak Source Current	$I_{HSGDSource}$	—	- 50	—	mA	R_{Load} = 10Ω+C_{Load} = 1nF [1)]
HSGD Peak Sink Current	$I_{HSGDSink}$	—	300	—	mA	R_{Load} = 10Ω+C_{Load} = 1nF [1)]
HSGD Rise Time	$T_{HSGDRise}$	120	220	300	ns	2V < V_{LSGD} < 8V R_{Load} = 10Ω+C_{Load} = 1nF
HSGD Fall Time	$T_{HSGDFall}$	19	35	70	ns	8V > V_{LSGD} > 2V R_{Load} = 10Ω+C_{Load} = 1nF

[1)] The parameter is not subject to Production Test – verified by Design / Characterization

3.6 Timer Section

Delay Timer 1	t_{TIMER1}	70	100	163.6	ms	For Fault Detection
Delay Timer 2	t_{TIMER2}	74	84	94	ms	For V_{BUS} > 95%
Inverter Time	t_{Inv}	100	130	163	µs	
Inverter Dead Time Max	$t_{DeadMax}$	0.85	1.05	1.25	µs	$V_{\_GD\_th}$ =2V R_{Load} = 10Ω+C_{Load} = 1nF
Inverter Dead Time Min	$t_{DeadMin}$	400	500	650	ns	$V_{\_GD\_th}$ =2V R_{Load} = 10Ω+C_{Load} = 1nF
Δ Inverter Dead Time Max	$t_{DeadMax}$	- 200	—	200	ns	
Δ Inverter Dead Time Min	$t_{DeadMin}$	- 200	—	200	ns	
Min. Duration of Sat. Control	$t_{Saturationmin}$	34	40	48	ms	
Max. Duration of Sat. Control	$t_{Saturationmax}$	197	—	236	ms	
Duration of Ext. Sat. Mode	tBLM	565	625	685	ms	

4 Application Example

4.1 Schematic

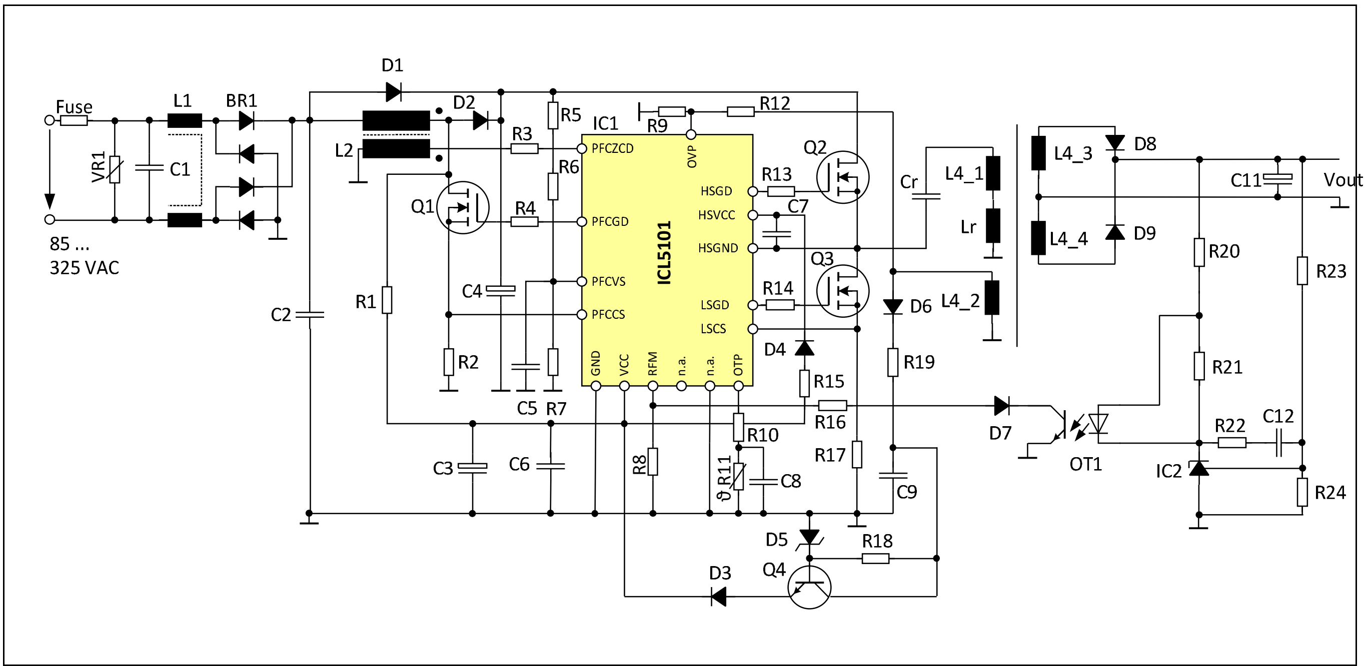


Figure 20 Schematic LED Driver using PFC / LLC Topology for 110W / 54V

5 Outline Dimensions

Outline dimensions are shown in .

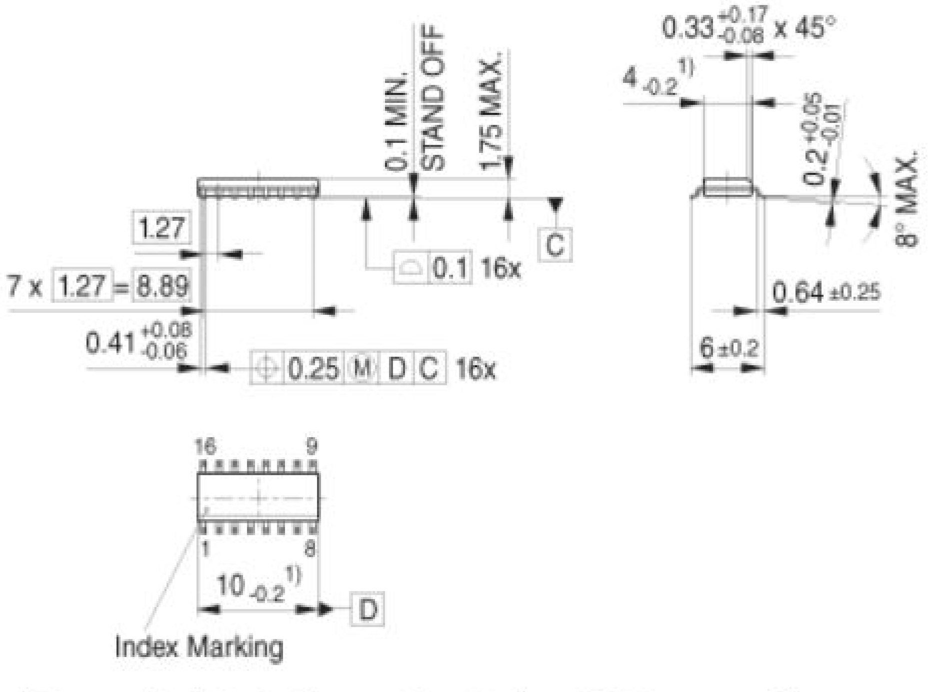


Figure 20 PG-DSO-16

Notes

1. *You can find all of our packages, sorts of packing and others in our Infineon Internet Page “Products”:* ***http://www.infineon.com/products****.*
2. *Dimensions in mm.*

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Page or Item	**Subjects (major changes since previous revision)**
Page 8 / 30 / 34	**RUN Frequency: 120 kHz @ - 40 °C / 130 kHz @ - 25 °C**
All	**Deleted Confidential**

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