Features

- **Low-voltage and Standard-voltage Operation**
  - **1.8 (V_{CC} = 1.8V to 5.5V)**
- **User-selectable Internal Organization**
  - **1K: 128 x 8 or 64 x 16**
- **Three-wire Serial Interface**
- **2 MHz Clock Rate (5V)**
- **Self-timed Write Cycle (5 ms max)**
- **High Reliability**
  - **Endurance: 1 Million Write Cycles**
  - **Data Retention: 100 Years**
- **8-lead JEDEC PDIP, 8-lead JEDEC SOIC, 8-lead Ultra Thin mini-MAP (MLP 2x3), 8-lead TSSOP and 8-ball dBGA2 Packages**
- **Die Sales: Wafer Form, Tape and Reel, and Bumped Wafers**

Description

The AT93C46D provides 1024 bits of serial electrically erasable programmable read-only memory (EEPROM), organized as 64 words of 16 bits each (when the ORG pin is connected to VCC), and 128 words of 8 bits each (when the ORG pin is tied to ground). The device is optimized for use in many industrial and commercial applications where low-power and low-voltage operations are essential. The AT93C46D is available in space-saving 8-lead PDIP, 8-lead JEDEC SOIC, 8-lead Ultra Thin mini-MAP (MLP 2x3), 8-lead TSSOP, and 8-lead dBGA2 packages.

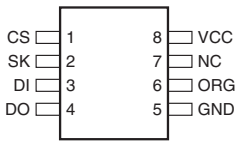
The AT93C46D is enabled through the Chip Select pin (CS) and accessed via a three-wire serial interface consisting of Data Input (DI), Data Output (DO), and Shift Clock (SK). Upon receiving a Read instruction at DI, the address is decoded and the data is clocked out serially on the DO pin. The Write cycle is completely self-timed, and no separate Erase cycle is required before Write. The Write cycle is only enabled when the part is in the Erase/Write Enable state. When CS is brought high following the initiation of a Write cycle, the DO pin outputs the Ready/Busy status of the part.

The AT93C46D is available in 1.8 (1.8V to 5.5V) version.

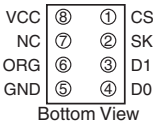
Table 0-1. Pin Configurations

Pin Name	Function
CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
GND	Ground
VCC	Power Supply
ORG	Internal Organization
NC	No Connect

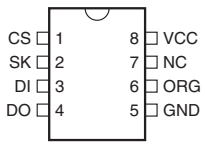
8-lead SOIC



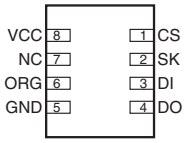
8-lead dBGA2



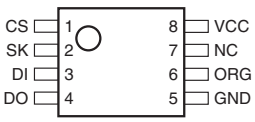
8-lead PDIP



8-lead Ultra Thin mini-MAP (MLP 2x3)



8-lead TSSOP



Three-wire Serial EEPROM

1K (128 x 8 or 64 x 16)

AT93C46D

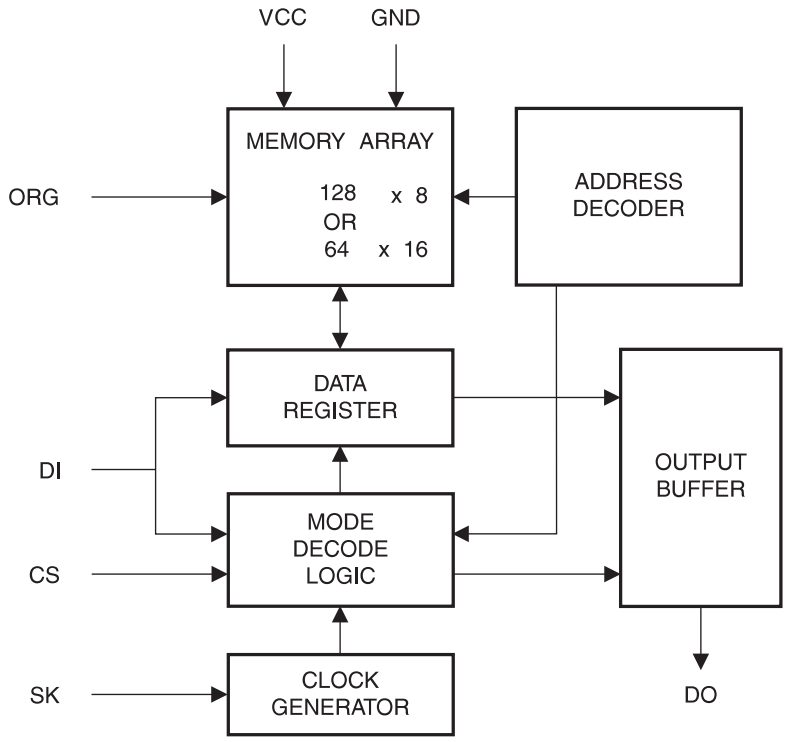
5193F–SEEPR–1/08

1. Absolute Maximum Ratings*

Operating Temperature	–55°C to +125°C
Storage Temperature	–65°C to +150°C
Voltage on Any Pin with Respect to Ground	–1.0V to +7.0V
Maximum Operating Voltage	6.25V
DC Output Current	5.0 mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

Figure 1-1. Block Diagram



Notes:
1. When the ORG pin is connected to VCC, the "x 16" organization is selected. When it is connected to ground, the "x 8" organization is selected. If the ORG pin is left unconnected and the application does not load the input beyond the capability of the internal 1 Meg ohm pullup, then the "x 16" organization is selected.
2. For the AT93C46D, if the "x 16" organization is the mode of choice and pin 6 (ORG) is left unconnected, Atmel® recommends using AT93C46E device. For more details, see the AT93C46E datasheet.

Table 1-1. Pin Capacitance[1]

Applicable over recommended operating range from T_A = 25°C, f = 1.0 MHz, V_{CC} = +1.8V (unless otherwise noted)

Symbol	Test Conditions	Max	Units	Conditions
C_{OUT}	Output Capacitance (DO)	5	pF	V_{OUT} = 0V
C_{IN}	Input Capacitance (CS, SK, DI)	5	pF	V_{IN} = 0V

Note: 1. This parameter is characterized and is not 100% tested.

Table 1-2. DC Characteristics

Applicable over recommended operating range from: T_{AI} = –40°C to +85°C, V_{CC} = +1.8V to +5.5V (unless otherwise noted)

Symbol	Parameter	Test Condition		Min	Typ	Max	Unit
V_{CC1}	Supply Voltage			1.8		5.5	V
V_{CC2}	Supply Voltage			2.7		5.5	V
V_{CC3}	Supply Voltage			4.5		5.5	V
I_{CC}	Supply Current	V_{CC} = 5.0V	READ at 1.0 MHz		0.5	2.0	mA
			WRITE at 1.0 MHz		0.5	2.0	mA
I_{SB1}	Standby Current	V_{CC} = 1.8V	CS = 0V		0.4	1.0	µA
I_{SB2}	Standby Current	V_{CC} = 2.7V	CS = 0V		6.0	10.0	µA
I_{SB3}	Standby Current	V_{CC} = 5.0V	CS = 0V		10.0	15.0	µA
I_{IL}	Input Leakage	V_{IN} = 0V to V_{CC}			0.1	1.0	µA
I_{OL}	Output Leakage	V_{IN} = 0V to V_{CC}			0.1	1.0	µA
V_{IL1}[1]	Input Low Voltage	2.7V ≤ V_{CC} ≤ 5.5V		–0.6		0.8	V
V_{IH1}[1]	Input High Voltage			2.0		V_{CC} + 1	
V_{IL2}[1]	Input Low Voltage	1.8V ≤ V_{CC} ≤ 2.7V		–0.6		V_{CC} x 0.3	V
V_{IH2}[1]	Input High Voltage			V_{CC} x 0.7		V_{CC} + 1	
V_{OL1}	Output Low Voltage	2.7V ≤ V_{CC} ≤ 5.5V	I_{OL} = 2.1 mA			0.4	V
V_{OH1}	Output High Voltage		I_{OH} = –0.4 mA	2.4			V
V_{OL2}	Output Low Voltage	1.8V ≤ V_{CC} ≤ 2.7V	I_{OL} = 0.15 mA			0.2	V
V_{OH2}	Output High Voltage		I_{OH} = –100 µA	V_{CC} – 0.2			V

Note: 1. V_{IL} min and V_{IH} max are reference only and are not tested.

Table 1-3. AC Characteristics

Applicable over recommended operating range from T_{AI} = –40°C to + 85°C, V_{CC} = +2.7V to +5.5V, CL = 1 TTL Gate and 100 pF (unless otherwise noted)

Symbol	Parameter	Test Condition		Min	Typ	Max	Units
f_{SK}	SK Clock Frequency	$4.5V \le V_{CC} \le 5.5V$ $2.7V \le V_{CC} \le 5.5V$ $1.8V \le V_{CC} \le 5.5V$		0 0 0		2 1 0.25	MHz
t_{SKH}	SK High Time	$4.5V \le V_{CC} \le 5.5V$ $2.7V \le V_{CC} \le 5.5V$ $1.8V \le V_{CC} \le 5.5V$		250 250 1000			ns
t_{SKL}	SK Low Time	$4.5V \le V_{CC} \le 5.5V$ $2.7V \le V_{CC} \le 5.5V$ $1.8V \le V_{CC} \le 5.5V$		250 250 1000			ns
t_{CS}	Minimum CS Low Time	$4.5V \le V_{CC} \le 5.5V$ $2.7V \le V_{CC} \le 5.5V$ $1.8V \le V_{CC} \le 5.5V$		250 250 1000			ns
t_{CSS}	CS Setup Time	Relative to SK	$4.5V \le V_{CC} \le 5.5V$ $2.7V \le V_{CC} \le 5.5V$ $1.8V \le V_{CC} \le 5.5V$	50 50 200			ns
t_{DIS}	DI Setup Time	Relative to SK	$4.5V \le V_{CC} \le 5.5V$ $2.7V \le V_{CC} \le 5.5V$ $1.8V \le V_{CC} \le 5.5V$	100 100 400			ns
t_{CSH}	CS Hold Time	Relative to SK		0			ns
t_{DIH}	DI Hold Time	Relative to SK	$4.5V \le V_{CC} \le 5.5V$ $2.7V \le V_{CC} \le 5.5V$ $1.8V \le V_{CC} \le 5.5V$	100 100 400			ns
t_{PD1}	Output Delay to “1”	AC Test	$4.5V \le V_{CC} \le 5.5V$ $2.7V \le V_{CC} \le 5.5V$ $1.8V \le V_{CC} \le 5.5V$			250 250 1000	ns
t_{PD0}	Output Delay to “0”	AC Test	$4.5V \le V_{CC} \le 5.5V$ $2.7V \le V_{CC} \le 5.5V$ $1.8V \le V_{CC} \le 5.5V$			250 250 1000	ns
t_{SV}	CS to Status Valid	AC Test	$4.5V \le V_{CC} \le 5.5V$ $2.7V \le V_{CC} \le 5.5V$ $1.8V \le V_{CC} \le 5.5V$			250 250 1000	ns
t_{DF}	CS to DO in High Impedance	AC Test CS = V_{IL}	$4.5V \le V_{CC} \le 5.5V$ $2.7V \le V_{CC} \le 5.5V$ $1.8V \le V_{CC} \le 5.5V$			100 150 400	ns
t_{WP}	Write Cycle Time		$1.8V \le V_{CC} \le 5.5V$	0.1	3	5	ms
Endurance[1]	5.0V, 25°C			1M			Write Cycles

Note: 1. This parameter is ensured by characterization.

Table 1-4. Instruction Set for the AT93C46D

Instruction	SB	Op Code	Address		Data		Comments
			x 8	x 16	x 8	x 16	
READ	1	10	$A_6 – A_0$	$A_5 – A_0$			Reads data stored in memory, at specified address
EWEN	1	00	11XXXXX	11XXXX			Write enable must precede all programming modes
ERASE	1	11	$A_6 – A_0$	$A_5 – A_0$			Erases memory location $A_n – A_0$
WRITE	1	01	$A_6 – A_0$	$A_5 – A_0$	$D_7 – D_0$	$D_{15} – D_0$	Writes memory location $A_n – A_0$
ERAL	1	00	10XXXXX	10XXXX			Erases all memory locations. Valid only at V_{CC} = 4.5V to 5.5V
WRAL	1	00	01XXXXX	01XXXX	$D_7 – D_0$	$D_{15} – D_0$	Writes all memory locations. Valid only at V_{CC} = 4.5V to 5.5V
EWDS	1	00	00XXXXX	00XXXX			Disables all programming instructions

Note: The Xs in the address field represent *DON'T CARE* values and must be clocked.

2. Functional Description

The AT93C46D is accessed via a simple and versatile three-wire serial communication interface. Device operation is controlled by seven instructions issued by the host processor. *A valid instruction starts with a rising edge of CS* and consists of a start bit (logic "1") followed by the appropriate op code and the desired memory address location.

READ (READ): The Read (READ) instruction contains the address code for the memory location to be read. After the instruction and address are decoded, data from the selected memory location is available at the serial output pin DO. Output data changes are synchronized with the rising edges of serial clock SK. It should be noted that a dummy bit (logic "0") precedes the 8- or 16-bit data output string.

ERASE/WRITE ENABLE (EWEN): To assure data integrity, the part automatically goes into the Erase/Write Disable (EWDS) state when power is first applied. An Erase/Write Enable (EWEN) instruction must be executed first before any programming instructions can be carried out. Please note that once in the EWEN state, programming remains enabled until an EWDS instruction is executed or V_{CC} power is removed from the part.

ERASE (ERASE): The Erase (ERASE) instruction programs all bits in the specified memory location to the logical "1" state. The self-timed erase cycle starts once the Erase instruction and address are decoded. The DO pin outputs the Ready/Busy status of the part if CS is brought high after being kept low for a minimum of 250 ns (t_{CS}). A logic "1" at pin DO indicates that the selected memory location has been erased and the part is ready for another instruction.

WRITE (WRITE): The Write (WRITE) instruction contains the 8 or 16 bits of data to be written into the specified memory location. The self-timed programming cycle t_{WP} starts after the last bit of data is received at serial data input pin DI. The DO pin outputs the Read/Busy status of the part if CS is brought high after being kept low for a minimum of 250 ns (t_{CS}). A logic "0" at DO indicates that programming is still in progress. A logic "1" indicates that the memory location at the specified address has been written with the data pattern contained in the instruction and the

part is ready for further instructions. *A Ready/Busy status cannot be obtained if the CS is brought high after the end of the self-timed programming cycle tWP.*

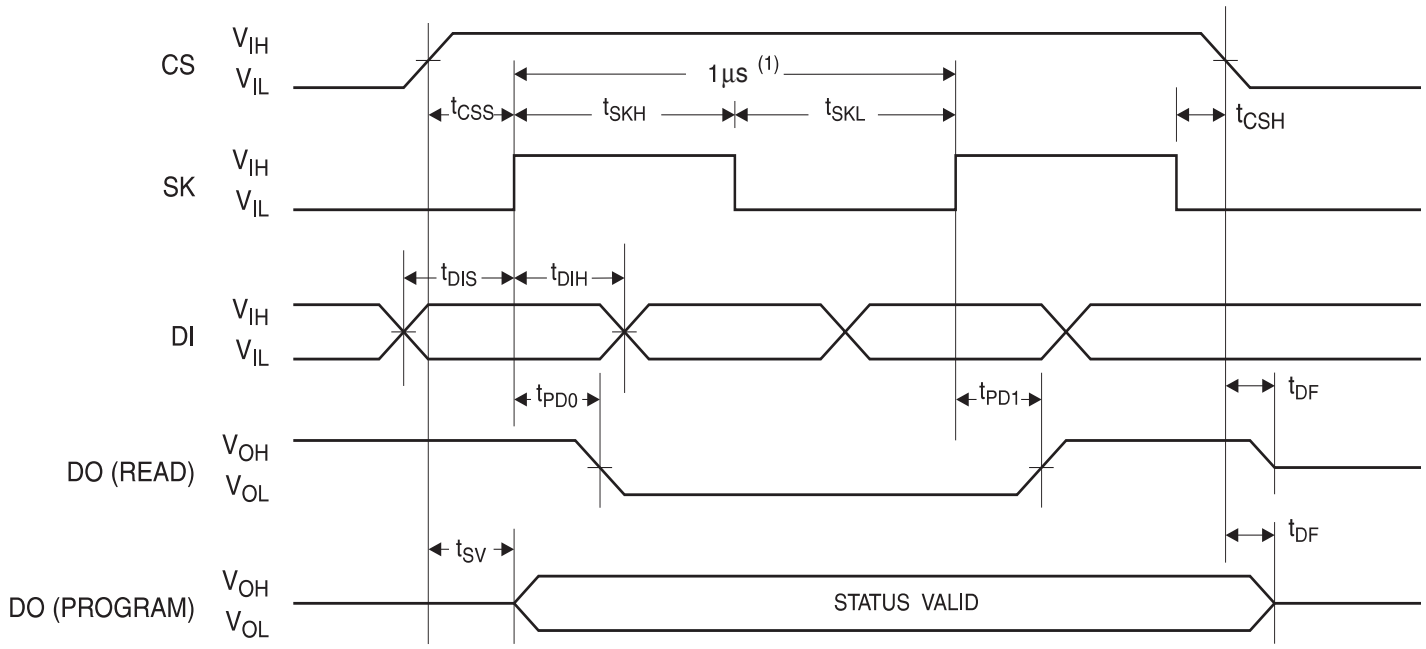
ERASE ALL (ERAL): The Erase All (ERAL) instruction programs every bit in the memory array to the logic "1" state and is primarily used for testing purposes. The DO pin outputs the Ready/Busy status of the part if CS is brought high after being kept low for a minimum of 250 ns (t_{CS}). The ERAL instruction is valid only at V_{CC} = 5.0V ± 10%.

WRITE ALL (WRAL): The Write All (WRAL) instruction programs all memory locations with the data patterns specified in the instruction. The DO pin outputs the Ready/Busy status of the part if CS is brought high after being kept low for a minimum of 250 ns (t_{CS}). The WRAL instruction is valid only at V_{CC} = 5.0V ± 10%.

ERASE/WRITE DISABLE (EWDS): To protect against accidental data disturb, the Erase/Write Disable (EWDS) instruction disables all programming modes and should be executed after all programming operations. The operation of the Read instruction is independent of both the EWEN and EWDS instructions and can be executed at any time.

3. Timing Diagrams

Figure 3-1. Synchronous Data Timing



Note: 1. This is the minimum SK period.

Table 3-1. Organization Key for Timing Diagrams

	AT93C46D (1K)	
I/O	**x 8**	**x 16**
A_N	A_6	A_5
D_N	D_7	D_{15}

Figure 3-2. READ Timing

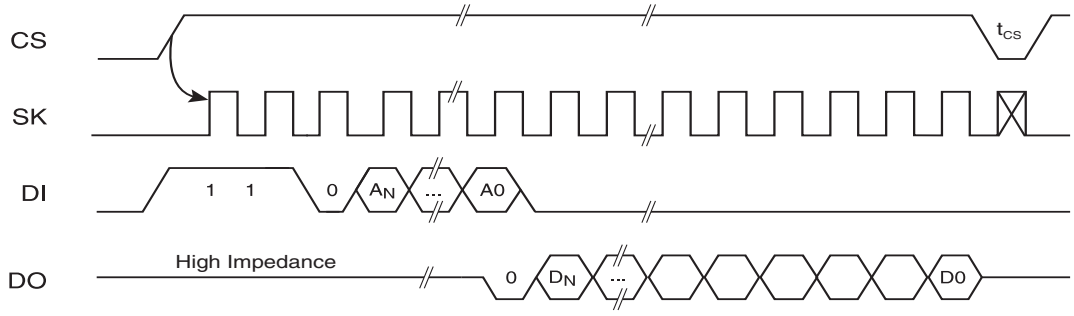


Figure 3-3. EWEN Timing

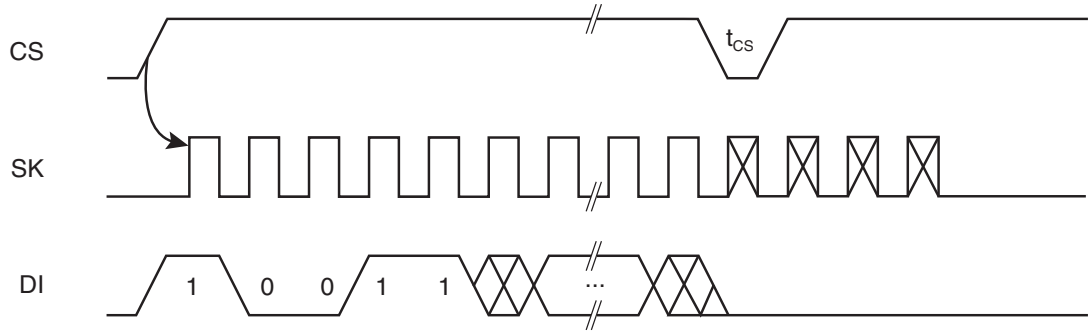


Figure 3-4. EWDS Timing

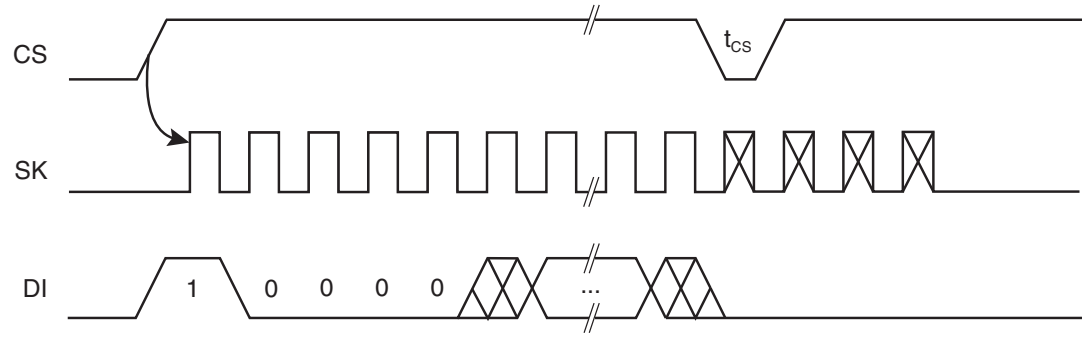


Figure 3-5. WRITE Timing

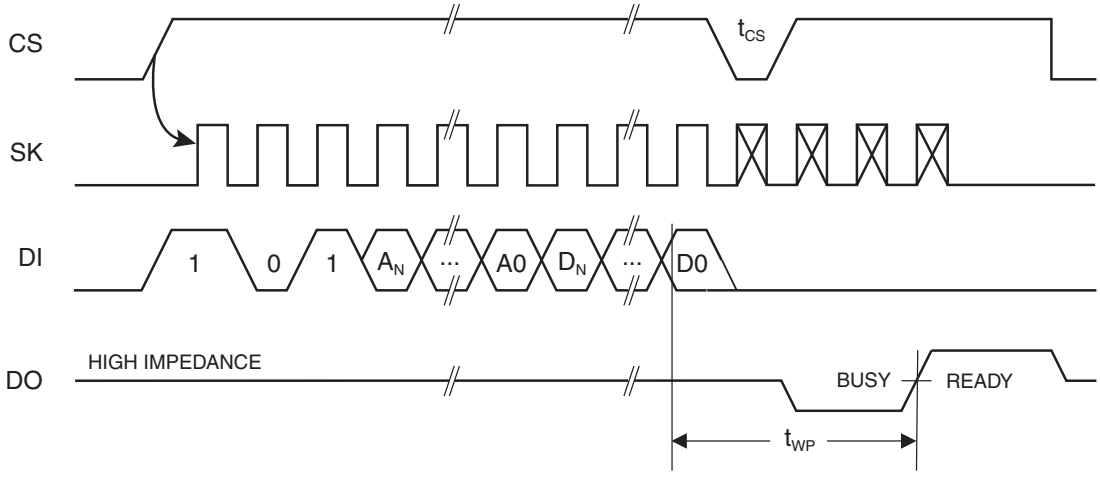
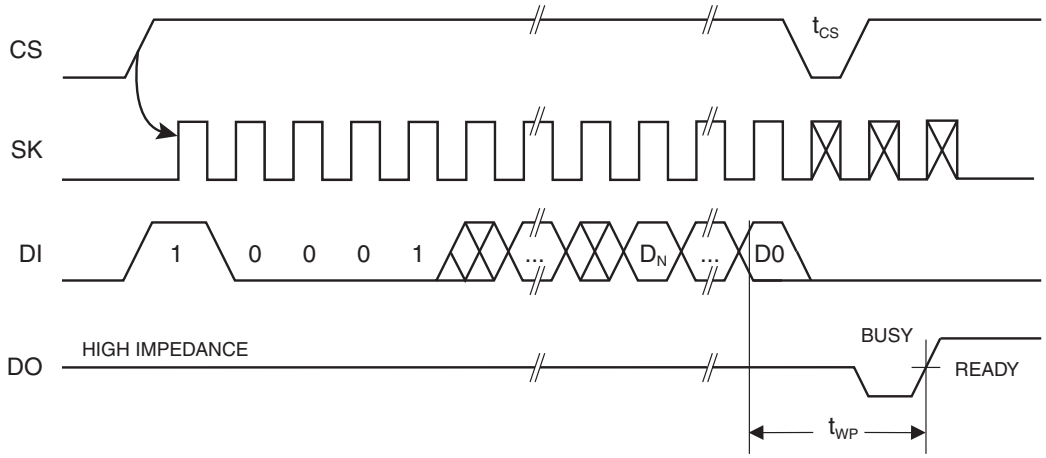


Figure 3-6. WRAL Timing[1]



Note: 1. Valid only at V_{CC} = 4.5V to 5.5V.

Figure 3-7. ERASE Timing

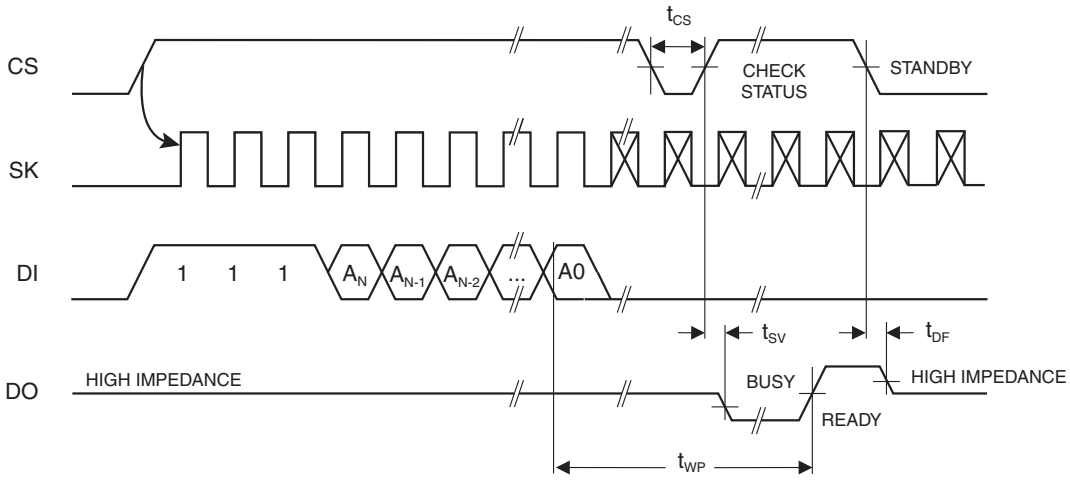
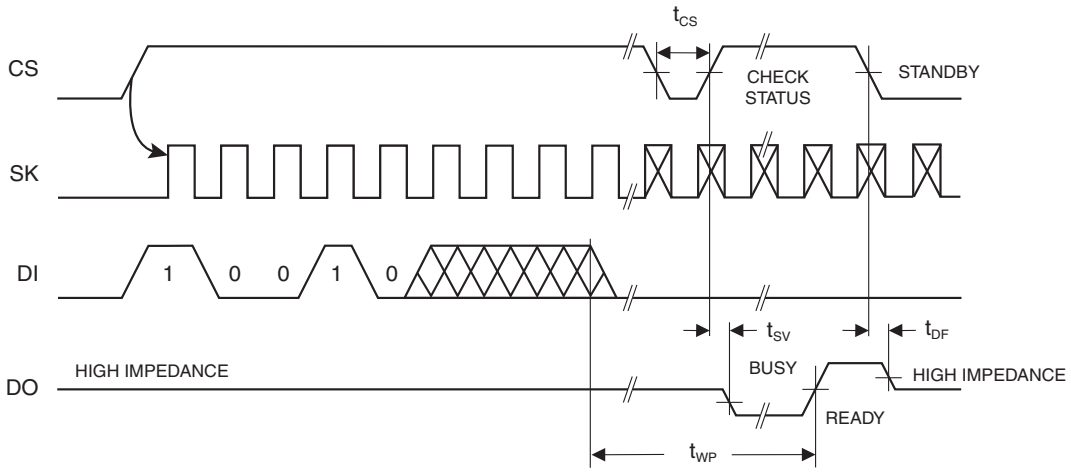


Figure 3-8. ERAL Timing[1]



Note: 1. Valid only at V_{CC} = 4.5V to 5.5V.

4. AT93C46D Ordering Information

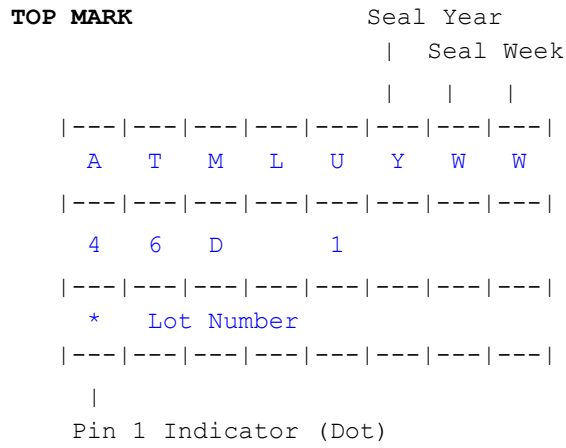
Ordering Code	Voltage	Package	Operation Range
AT93C46D-PU (Bulk form only)	1.8	8P3	Lead-free/Halogen-free/ Industrial Temperature (−40°C to 85°C)
AT93C46DN-SH-B[1] (NiPdAu Lead finish)	1.8	8S1	
AT93C46DN-SH-T[2] (NiPdAu Lead finish)	1.8	8S1	
AT93C46D-TH-B[1] (NiPdAu Lead finish)	1.8	8A2	
AT93C46D-TH-T[2] (NiPdAu Lead finish)	1.8	8A2	
AT93C46DY6-YH-T[2] (NiPdAu Lead finish)	1.8	8Y6	
AT93C46DU3-UU-T[2]	1.8	8U3-1	
AT93C46D-W-11[3]	1.8	Die Sale	Industrial (−40°C to 85°C)

Notes:
1. "-B" denotes bulk
2. "-T" denotes tape and reel. SOIC = 4K per reel. TSSOP, Ultra Thin Mini MAP, and dBGA2 = 5K per reel.
3. Available in tape and reel, and wafer form; order as SL788 for inkless wafer form. Bumped die available upon request. Please contact Serial Interface Marketing.

Package Type	
8P3	8-lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
8S1	8-lead, 0.150" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
8A2	8-lead, 0.170" Wide, Thin Shrink Small Outline Package (TSSOP)
8U3-1	8-ball, Die Ball Grid Array Package (dBGA2)
8Y6	8-lead, 2.00 mm x 3.00 mm Body, 0.50mm Pitch, Ultra-Thin Mini-MAO, Dual No Lead Package. (DFN), (MLP 2x3mm)
Options	
–1.8	Low Voltage (1.8V to 5.5V)

5. Part Marking Scheme

5.1 AT93C46D 8-PDIP



Y = SEAL YEAR

6: 2006 0: 2010
7: 2007 1: 2011
8: 2008 2: 2012
9: 2009 3: 2013

WW = SEAL WEEK

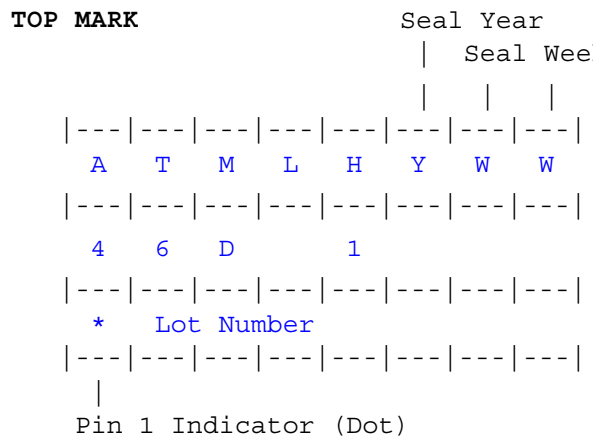
02 = Week 2
04 = Week 4
:: : :::: :
:: : :::: ::
50 = Week 50
52 = Week 52

Lot Number to Use ALL Characters in Marking

BOTTOM MARK

No Bottom Mark

5.2 AT93C46D 8-SOIC



Y = SEAL YEAR

6: 2006 0: 2010
7: 2007 1: 2011
8: 2008 2: 2012
9: 2009 3: 2013

WW = SEAL WEEK

02 = Week 2
04 = Week 4
:: : :::: :
:: : :::: ::
50 = Week 50
52 = Week 52

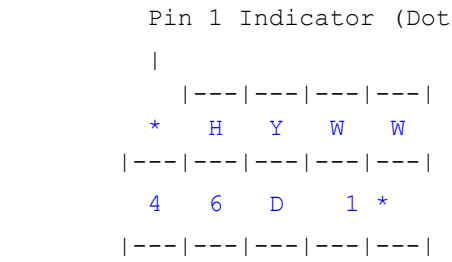
Lot Number to Use ALL Characters in Marking

BOTTOM MARK

No Bottom Mark

5.3 AT93C46D 8-TSSOP

TOP MARK



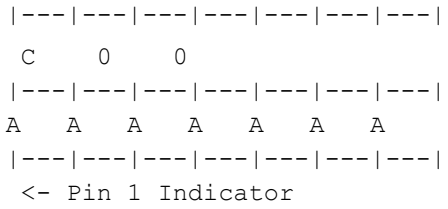
Y = SEAL YEAR

6: 2006
7: 2007
8: 2008
9: 2009
0: 2010
1: 2011
2: 2012
3: 2013

WW = SEAL WEEK

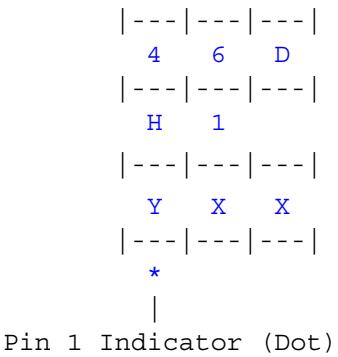
02 = Week 2
04 = Week 4
:: : :::: :
:: : :::: ::
50 = Week 50
52 = Week 52

BOTTOM MARK



5.4 AT93C46D 8-Ultra Thin Mini MAP

TOP MARK



Y = YEAR OF ASSEMBLY

XX = ATMEL LOT NUMBER TO COORESPOND WITH NSEB TRACE CODE LOG BOOK.
(e.g. XX = AA, AB, AC,...AX, AY, AZ)

Y = SEAL YEAR

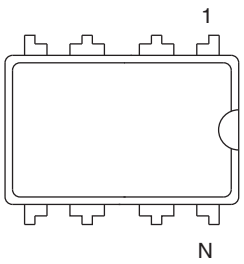
6: 2006
7: 2007
8: 2008
9: 2009
0: 2010
1: 2011
2: 2012
3: 2013

5.5 AT93C46D dBGA2

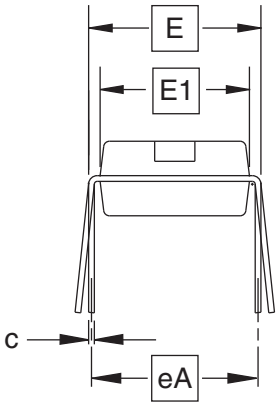
```
TOP MARK

LINE 1------->     46DU
LINE 2------->     YMTC
                  |<--  Pin 1 This Corner

 Y = ONE DIGIT YEAR CODE
4: 2004   7: 2007
5: 2005   8: 2008
6: 2006   9: 2009

M = SEAL MONTH (USE ALPHA DESIGNATOR A-L)
 A = JANUARY
 B = FEBRUARY
 " " """""""
 J = OCTOBER
 K = NOVEMBER
 L = DECEMBER

   TC = TRACE CODE (ATMEL LOT
   NUMBERS TO CORRESPOND
   WITH ATK TRACE CODE LOG BOOK)
```

6. Package Information

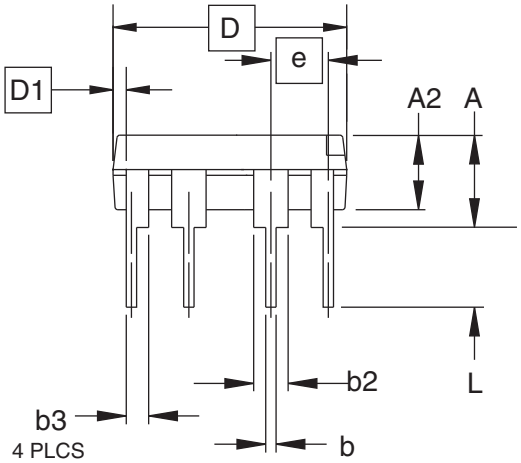
8P3 - PDIP



Top View



End View



Side View

COMMON DIMENSIONS
(Unit of Measure = inches)

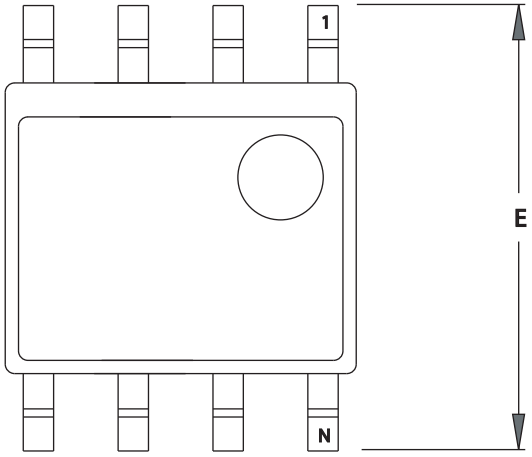
SYMBOL	MIN	NOM	MAX	NOTE
A			0.210	2
A2	0.115	0.130	0.195	
b	0.014	0.018	0.022	5
b2	0.045	0.060	0.070	6
b3	0.030	0.039	0.045	6
c	0.008	0.010	0.014	
D	0.355	0.365	0.400	3
D1	0.005			3
E	0.300	0.310	0.325	4
E1	0.240	0.250	0.280	3
e	0.100 BSC			
eA	0.300 BSC			4
L	0.115	0.130	0.150	2

Notes:
1. This drawing is for general information only; refer to JEDEC Drawing MS-001, Variation BA for additional information.
2. Dimensions A and L are measured with the package seated in JEDEC seating plane Gauge GS-3.
3. D, D1 and E1 dimensions do not include mold Flash or protrusions. Mold Flash or protrusions shall not exceed 0.010 inch.
4. E and eA measured with the leads constrained to be perpendicular to datum.
5. Pointed or rounded lead tips are preferred to ease insertion.
6. b2 and b3 maximum dimensions do not include Dambar protrusions. Dambar protrusions shall not exceed 0.010 (0.25 mm).

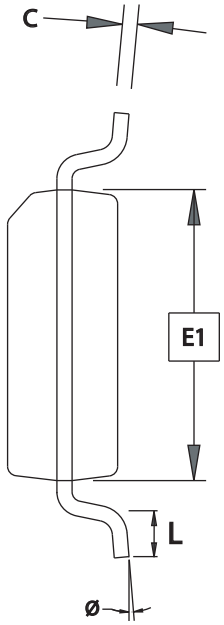
01/09/02

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**8P3**, 8-lead, 0.300" Wide Body, Plastic Dual In-line Package (PDIP)	8P3	B

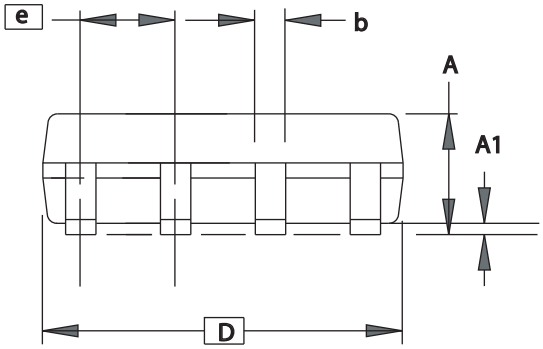
8S1 - JEDEC SOIC



TOP VIEW



END VIEW



SIDE VIEW

COMMON DIMENSIONS
(Unit of Measure = mm)

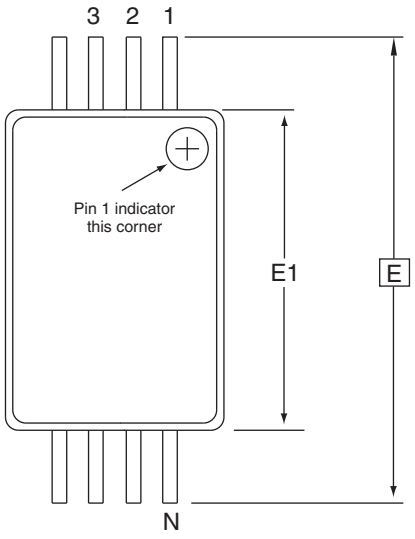
SYMBOL	MIN	NOM	MAX	NOTE
A	1.35	–	1.75	
A1	0.10	–	0.25	
b	0.31	–	0.51	
C	0.17	–	0.25	
D	4.80	–	5.05	
E1	3.81	–	3.99	
E	5.79	–	6.20	
e	1.27 BSC			
L	0.40	–	1.27	
θ	0°	–	8°	

Note: These drawings are for general information only. Refer to JEDEC Drawing MS-012, Variation AA for proper dimensions, tolerances, datums, etc.

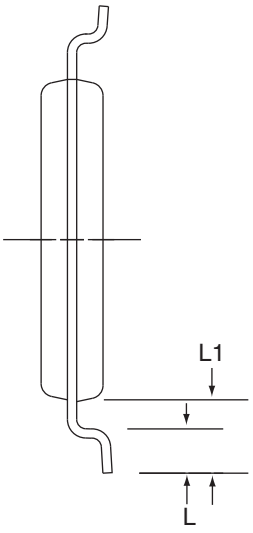
3/17/05

	TITLE	DRAWING NO.	REV.
1150 E. Cheyenne Mtn. Blvd. Colorado Springs, CO 80906	8S1, 8-lead (0.150" Wide Body), Plastic Gull Wing Small Outline (JEDEC SOIC)	8S1	C

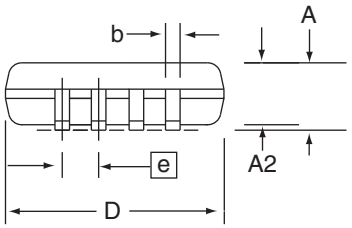
8A2 - TSSOP



Top View



End View



Side View

COMMON DIMENSIONS
(Unit of Measure = mm)

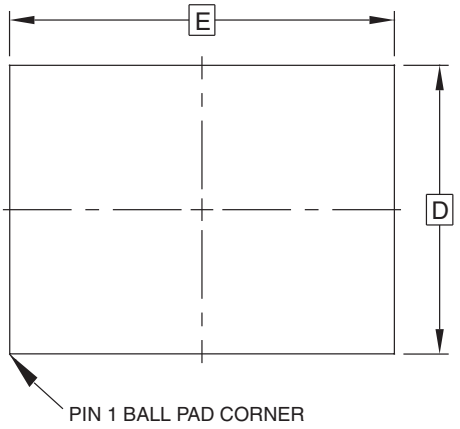
SYMBOL	MIN	NOM	MAX	NOTE
D	2.90	3.00	3.10	2, 5
E		6.40 BSC		
E1	4.30	4.40	4.50	3, 5
A	–	–	1.20	
A2	0.80	1.00	1.05	
b	0.19	–	0.30	4
e		0.65 BSC		
L	0.45	0.60	0.75	
L1		1.00 REF		

Notes:
1. This drawing is for general information only. Refer to JEDEC Drawing MO-153, Variation AA, for proper dimensions, tolerances, datums, etc.
2. Dimension D does not include mold Flash, protrusions or gate burrs. Mold Flash, protrusions and gate burrs shall not exceed 0.15 mm (0.006 in) per side.
3. Dimension E1 does not include inter-lead Flash or protrusions. Inter-lead Flash and protrusions shall not exceed 0.25 mm (0.010 in) per side.
4. Dimension b does not include Dambar protrusion. Allowable Dambar protrusion shall be 0.08 mm total in excess of the b dimension at maximum material condition. Dambar cannot be located on the lower radius of the foot. Minimum space between protrusion and adjacent lead is 0.07 mm.
5. Dimension D and E1 to be determined at Datum Plane H.

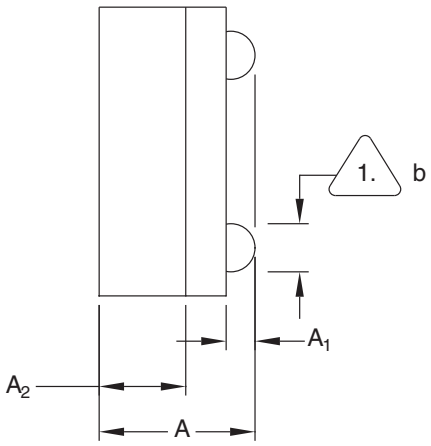
5/30/02

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**8A2**, 8-lead, 4.4 mm Body, Plastic Thin Shrink Small Outline Package (TSSOP)	8A2	B

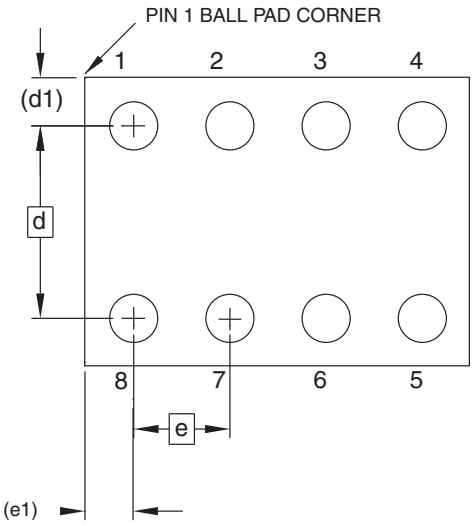
8U3-1 – dBGA2



Top View



Side View



Bottem View
8 SOLDER BALLS

1. This drawing is for general information only.
2. Dimension 'b' is measured at maximum solder ball diameter.

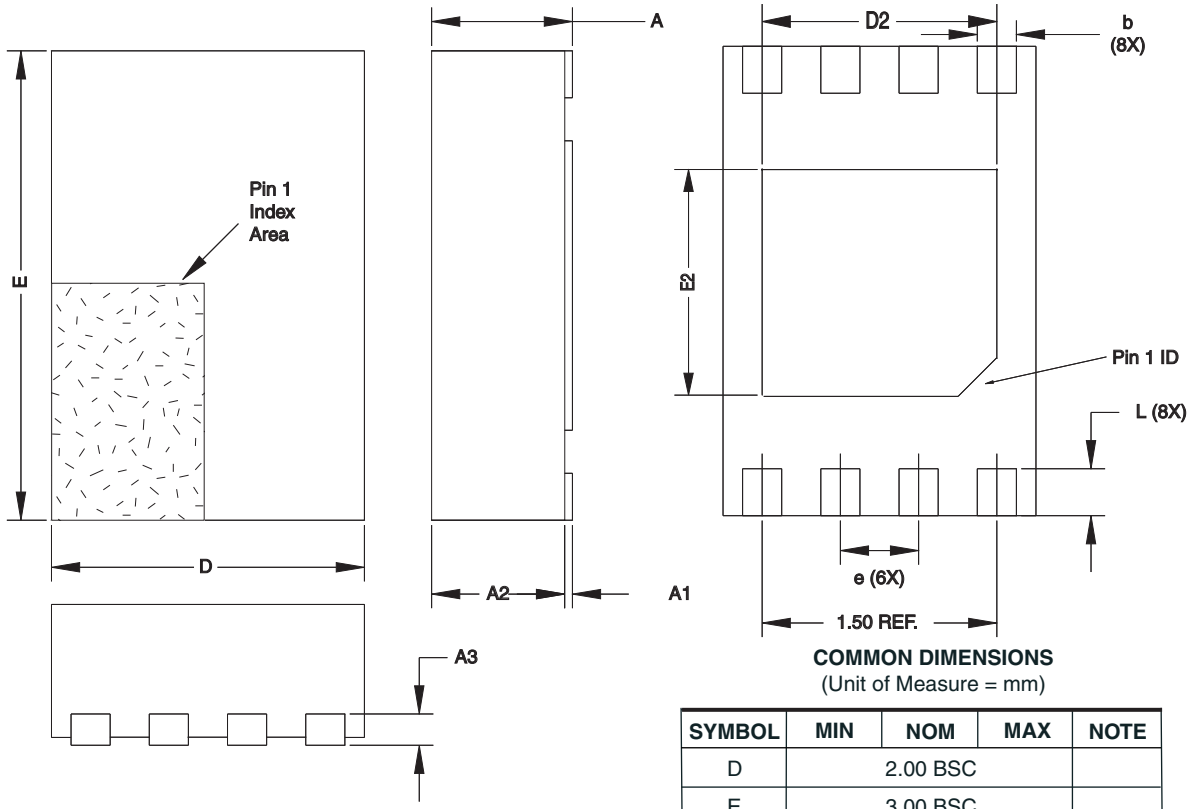
COMMON DIMENSIONS
(Unit of Measure - mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	0.73	0.79	0.85	
A1	0.09	0.14	0.19	
A2	0.40	0.45	0.50	
b	0.20	0.25	0.30	2
D	1.50 BSC			
E	2.0 BSC			
e	0.50 BSC			
e1	0.25 REF			
d	1.00 BSC			
d1	0.25 REF			

5/3/05

	TITLE	DRAWING NO.	REV.
1150 E. Cheyenne Mtn. Blvd. Colorado Springs, CO 80906	**8U3-1**, 8-ball, 1.50 x 2.00 mm Body, 0.50 mm pitch, Small Die Ball Grid Array Package (dBGA2)	PO8U3-1	B

8Y6 – MLP 2x3



COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
D		2.00 BSC		
E		3.00 BSC		
D2	1.40	1.50	1.60	
E2	-	-	1.40	
A	-	-	0.60	
A1	0.0	0.02	0.05	
A2	-	-	0.55	
A3		0.20 REF		
L	0.20	0.30	0.40	
e		0.50 BSC		
b	0.20	0.25	0.30	2

Notes:
1. This drawing is for general information only. Refer to JEDEC Drawing MO-229, for proper dimensions, tolerances, datums, etc.
2. Dimension b applies to metallized terminal and is measured between 0.15 mm and 0.30 mm from the terminal tip. If the terminal has the optional radius on the other end of the terminal, the dimension should not be measured in that radius area.
3. Soldering the large thermal pad is optional, but not recommended. No electrical connection is accomplished to the device through this pad, so if soldered it should be tied to ground

10/16/07

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**8Y6**, 8-lead 2.0 x 3.0 mm Body, 0.50 mm Pitch, Utlra Thin Mini-Map, Dual No Lead Package (DFN) ,(MLP 2x3)	8Y6	D

7. Revision History

Doc. Rev.	Date	Comments
5193F	1/2008	Removed ‘preliminary’ status
5193E	11/2007	Modified ‘max’ value in AC Characteristics table
5193D	8/2007	Moved Pinout figure Added new feature for Die Sales Modified Ordering Information table layout Modified Park Marking Schemes
5193C	6/2007	Updated to new template Added Product Markup Scheme Added Technical email contact
5193C	3/2007	Corrected Figures 4 and 5.
5193B	2/2007	Added ‘Ultra Thin’ description to 8-lead Mini-MAP package.
5193A	1/2007	Initial document release.

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